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(54) **TEOS based plasma enhanced chemical vapor deposition process for deposition of silicon dioxide films.**

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Description

The present invention relates to TEOS based, plasma enhanced, CVD processes for depositing films of silicon oxide.

I. Reactor

The early gas chemistry deposition reactors that were applied to semiconductor integrated circuit fabrication used relatively high temperature, thermally-activated chemistry to deposit from a gas onto a heated substrate. Such chemical vapor deposition of a solid onto a surface involves a heterogeneous surface reaction of gaseous species that absorb onto the surface. The rate of film growth and the film quality depend on the water surface temperature and on the gaseous species available.

More recently, low temperature plasma-enhanced deposition and etching techniques have been developed for forming diverse materials, including metals such as aluminium and tungsten, dielectric films such as silicon nitride and silicon dioxide, and semiconductor films such as silicon.

The plasma used in the available plasma-enhanced chemical vapor deposition processes is a low pressure reactant gas discharge which is developed in an RF field. The plasma is, by definition, an electrically neutral ionized gas in which there are equal number densities of electrons and ions. At the relatively low pressure used in PECVD, the discharge is in the "glow" region and the electron energies can be quite high relative to heavy particle energies. The very high electron temperatures increase the density of disassociated species within the plasma which are available for deposition on nearby surfaces (such as substrates). The enhanced supply of reactive free radicals in the PECVD processes makes possible the deposition of dense, good quality films at lower temperatures and at faster deposition rates 30 to 40 nm/min. (300 to 400 Angstroms per minute) than are typically possible using purely thermally-activated CVD processes 10 to 20 nm/min. (100 to 200 Angstroms per minute). However the deposition rates available using conventional plasma-enhanced processes are still relatively low.

Presently, batch-type reactors are used in most commercial PECVD applications. The batch reactors process a relatively large number of wafers at once and, thus, provide relatively high throughput despite the low deposition rates. However, single-wafer reactors have certain advantages, such as the lack of within-batch uniformity problems, which make such reactors attractive, particularly for large, expensive wafers such as 12.7 to 20.32 cm (5-8 inch) diameter wafers. In addition, and quite obviously, increasing the deposition rate and throughput of such single wafer reactors would further increase their range of useful applications.

II. Thermal CVD of SiO$_2$; Planarization Process

Recently, integrated circuit (IC) technology has advanced from large scale integration (LSI) to very large scale integration (VLSI) and is projected to grow to ultra-large integration (ULSI) over the next several years. This advancement is monolithic circuit integration has been made possible by improvements in the manufacturing equipement as well as in the materials and methods used in processing semiconductor wafers into IC chips. However, the incorporation into IC chips of, first, increasingly complex devices and circuits and, second, greater device densities and smaller separations, imposes increasingly stringent requirements on the basic integrated circuit fabrication steps of masking, film formation, doping and etching.

As an example of the increasing complexity, it is projected that, shortly, typical MOS (metal oxide semiconductor) memory circuits will contain two levels of metal interconnect layers, while MOS logic circuits may well use two to three metal interconnect layers and bipolar digital circuits may require three to four such layers. The increasing complexity, thickness/depth and small size of such multiple interconnect levels make it increasingly difficult to fabricate the required conformal, planar interlevel dielectric layers materials such as silicon dioxide that support and electrically isolate such metal interconnect layers.

The difficulty in forming planarized conformal coatings on small stepped surface topographies is illustrated in FIG. 16. There, a first film such as a conductor layer 171 has been formed over the existing stepped topography of a partially completed integrated circuit (not shown) and is undergoing the deposition of an interlayer dielectric layer 172 such as silicon dioxide. This is done preparatory to the formation of a second level conductor layer (not shown). Typically, where the mean-free path of the depositing active species is long compared to the step dimensions and where there is no rapid surface migration, the deposition rates at the bottom 173, the sides 174 and the top 175 of the stepped topography are proportional to the associated arrival angles. The bottom and side arrival angles are a function of and are limited by the depth and small width of the trench. Thus, for very narrow and/or deep geometries the thickness of the bottom layer 173 tends to be deposited to a lesser thickness than is the side layer 174 which, in turn, is less than the thickness of top layer 175.

Increasing the pressure used in the deposition process typically will increase the collision rate of

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the active species and decrease the mean-free path. This would increase the arrival angles and, thus, increase the deposition rate at the sidewalls 174 and bottom 173 of the trench or step. However, and referring to FIG. 17A, this also increases the arrival angle and associated deposition rate at stepped corners 176.

For steps separated by a wide trench, the resulting inwardly sloping film configuration forms cusps 177-177 at the sidewall-bottom interface. It is difficult to form conformal metal and/or dielectric layers over such topographies. As a consequence, it is necessary to separately planarize the topography.

In addition, and referring to FIG. 17B, where the steps are separated by a narrow trench, for example, in dense 256 kilobit VLSI structures, the increased deposition rate at the corner 176 encloses a void 178. Such voids are exposed by subsequent planarization procedures and may allow the second level conductor to penetrate and run along the void and short the conductors and devices along the void.

THIN SOLID FILMS, Vol.97, No. 1, Pages 53 to 61, Lausanne, Switzerland discloses silicon dioxide gate insulators prepared at near room temperature on InSb by plasma-enhanced chemical vapour deposition from tetraethoxysilane (TEOS) in an oxygen plasma. The films are characterised by ellipsometry and IR Fourier spectroscopy. The predominant chemical component is SiO_2, with some impurities, such as hydrocarbon groups and water. The objective was the preparation of high quality gate oxides for metal/oxide/semiconductor (MOS) studies. The MOS performance of the films is demonstrated with capacitance-voltage curves, breakdown field strengths and film resistivity measurements. Inversion carrier mobilities on p-type InSb of up to $70000 cm^2 V^{-1}s^{-1}$ at liquid helium temperature have been achieved.

ELECTROCHEMICAL TECHNOLOGY, Vol.6, No. 7/8, 8th July 1968, Pages 251 to 256, Princetown, New Jersey, U.S.A. discloses the effects of environmental conditions on SiO_2 from room temperature up to $800 \cdot C$ for films which have been chemically vapor plated by the reaction of oxygen and tetraethyl orthosilicate with a view toward using these oxides in germanium device technology. The results fall into two categories, namely: 1) those relating to the bulk properties of the film, and 2) those occurring through changes at the substrate - SiO_2 interface. Bulk effects were monitored by etch rate, infrared absorption and dielectric measurements. These properties are significantly affected by dry atmospheres only at temperatures of the order of $800 \cdot C$, in which case the changes indicate densification. It is found that the addition of moisture to the atmosphere results in comparable den-

sification at $450 \cdot C$. Exposure to high humidity at room temperature, which is too low a temperature to yield significant densification, results in an increased dielectric constant and dissipation factor for previously undensified oxides, but has no such effect on densified samples. The effects related to the oxide-substrate interface are cracking and flaking of the film, and occur on germanium substrates, but not on silicon or sapphire. Cracking results from exposure to temperatures above about $700 \cdot C$ when the oxide thickness exceeds 3000-4000A. Thinner films exhibit similar cracking at this temperature if they have been previously subject to wet densification at $450 \cdot C$. Also, storage in high humidity at room temperature leads to cracking and flaking within a few weeks and is accompanied by the formation of GeO_2. It is concluded that the oxide films studied are permeable to water unless densified at $800 \cdot C$, and that the oxygen-tetraethyl orthosilicate reaction is therefore undesirable as a low-temperature process for semiconductor device technology.

This invention provides a TEOS-based, plasma enhanced, CVD process for depositing a film of a silcon oxide having improved step coverage onto a surface of a semiconductor wafer having small dimension stepped topographics, such wafer being positioned inside a vacuum chamber to receive the silicon oxide, comprising the steps of:

heating the wafer to a temperature in the range of about $200 \cdot C$-$500 \cdot C$;

pressurizing the chamber to between about 133.322 Pa to 6666 Pa (1 to 50 Torr);

dispensing toward the wafer a gas mixture which includes an effective amount of tetraethylorthosilicate ("TEOS") from a dispensing area which is close to the wafer surface, the gas mixture being dispensed with a substantially uniform spatial distribution over the wafer surface; and

applying an effective amount of RF power between the dispensing area and the wafer, so as to excite the gas mixture into a plasma state in a thin region between the wafer and the dispensing area;

whereby a layer of silicon oxide having improved step coverage is deposited onto the wafer.

Preferably oxygen is provided to the gas mixture at an oxygen flow rate between about $100 \times 10^{-6} m^3$/min. and $1000 \times 10^{-6} m^3$/min. (100 and 1000 sccm) such that the total flow rate of the gas mixture is between $200 \times 10^{-6} m^3$/min. and $2500 \times 10^{-6} m^3$/min. (200 and 2500 sccm).

It is also preferred that RF power is carried out at a density of about 1 watt/cm^2.

By way of example the RF power may be supplied via terminals, one of the terminals for said RF power supply being coupled to said wafer.

More specifically the step of applying RF power may be carried out at a frequency of approxi-

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mately 13.56 MHz.

According to a further feature of the invention the step of applying said RF power may include confining the plasma to a region corresponding to a single wafer.

For example the gas mixture may be dispensed from a generally planar dispensing area which is located close to and substantially parallel with the wafer surface. In particular the surface area of said planar dispensing area may be approximately equal to or greater than the surface area of said wafer surface.

The process may further include the step of gasifying liquid TEOS.

In accordance with a further feature of the invention the process may include the step of transporting the wafer to its position in the chamber close to and substantially parallel to the planar dispensing region.

In one specific process according to the invention the process may include the steps of: positioning the substrate on a support within a vacuum chamber; communicating the gas mixture onto the chamber to a first volume adjacent the substrate; directing the gas mixture from said first volume in a multiplicity of closely-spaced streams through a second volume between the first volume and the substrate while applying RF energy to the second volume: and maintaining the total pressure in the chamber within the range of about 133.322 Pa to 6666 Pa (1 to 50 Torr) and the temperature of the substrate in the range of about 200 °C to 500 °C.

In the latter case the chamber may be pressurised to between about 133.322 Pa to 1600 Pa (1 to 12 Torr).

The process may also include the step of confining the plasma created to a region corresponding to a single wafer.

Said dispensing step may further comprise dispensing the gas mixture toward the wafer through a plurality of openings in an electrically conductive electrode, said dispensing electrode having a planar surface containing said openings which faces the wafer and which is substantially coextensive with said planar dispensing area; and wherein the step of applying RF power further comprises electrically connecting a source of RF power to the dispensing electrode.

The following is a description of some specific embodiments of the invention with reference being made to the following drawing figures, in which:

FIG. 1 is a top plan view of a combined CVD/PECVD reactor for use in performing the present invention, shown with the cover pivoted open;

FIG. 2 is a vertical cross-section, partly in schematic, taken along line 2-2 in FIG. 1, with the reactor cover closed;

FIG. 3 is a vertical cross-section through the wafer elevator mechanism, taken along line 3-3 in FIG. 1;

FIGS. 4-8 are sequential, highly schematized representations of the operation of the wafer transport system in positioning wafers within, and removing wafers from the reactor susceptor;

FIG. 9 is a reduced scale, horizontal cross-section through the circular-array, radiant lamp heating assembly, taken along line 9-9 in FIG. 2;

FIG. 10 is an enlarged, partial depiction of FIG. 2 showing the process gas and purge gas distribution systems in greater detail;

FIG. 11 is a partial, enlarged bottom plan view of the gas distribution head or manifold;

FIG. 12 depicts an enlarged, vertical cross-section of the RF/gas feed-through system shown in FIG. 2;

FIGS. 13A-13C schematically depict various alternative embodiments of the gas feed-through;

FIG. 14 illustrates breakdown voltage as a function of pressure for low frequency and high frequency RF power without a constant voltage gradient device;

FIG. 15 illustrates breakdown voltage as a function of pressure with and without a constant voltage gradient device;

FIG. 16 is a schematic cross-sectional representation of an integrated circuit which illustrates the arrival angles associated with the deposition of a layer of material such as dielectric onto a surface of stepped topography;

FIGS. 17A and 17B are schematic cross-sections, similar to FIG. 16, which illustrate the effect of trench width on planarization;

FIGS. 18 and 19 are cross-sections of the surface topology of an integrated circuit, in the manner of FIG. 16, illustrating the conformal, planar qualities of oxide films resulting from the application of our planarization process; and

FIGS. 20 and 21 depict the deposition rate as a function of temperature and pressure, respectively, for our present oxide deposition process.

I. CVD/PECVD Reactor

A. Overview of CVD/PECVD Reactor

FIGS. 1 and 2 are, respectively, a top plan view of the single wafer reactor 10 for performing the process of the present invention shown with the cover pivoted open, and a vertical cross-section of the reactor 10.

Referring primarily to these two figures and to others indicated parenthetically, the reactor system 10 comprises a housing 12 (also termed a "chamber"), typically made of aluminum, which defines an inner vacuum chamber 13 that has a plasma

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processing region 14 (FIG. 6). The reactor system 10 also includes a wafer-holding susceptor 16 and a unique wafer transport system 18 (FIG. 1) that includes vertically movable wafer support fingers 20 and susceptor support fingers 22. These fingers cooperate with an external robotic blade 24 (FIG. 1) for introducing wafers 15 into the process region or chamber 14 and depositing the wafers 15 on the susceptor 16 for processing, then removing the wafers 15 from the susceptor 16 and the chamber 12. The reactor system 10 further comprises a process/purge gas manifold or "box" 26 that applies process gas and purging gas to the chamber 13, an RF power supply and matching network 28 for creating and sustaining a process gas plasma from the inlet gas and a lamp heating system 30 for heating the susceptor 16 and wafer 15 positioned on the susceptor to effect deposition onto the wafer. Preferably, high frequency RF power of 13.56 MHz is used, but low frequencies can be used.

The gas manifold 26 is part of a unique process and purge gas distribution system 32 (FIGS. 2 and 10) that is designed to flow the process gas evenly radially outwardly across the wafer 15 to promote even deposition across the wafer and to purge the spent gas and entrained products radially outwardly from the edge of the wafer 15 at both the top and bottom thereof to substantially eliminate deposition on (and within) the gas manifold or box 26 and the chamber 12.

A liquid cooling system 34 controls the temperature of the components of the chamber 12 including, in particular, the temperature of the gas manifold or box 26. The temperature of the gas box components is selected to eliminate premature deposition within the gas box/manifold 26 upstream from the process chamber 14.

The reactor system 10 includes a unique, RF/gas feed-through device 36 (FIGS. 2 and 12) that supplies process and purge gas to the RF-driven gas manifold 26 from an electrically ground supply. Applying the RF energy to the gas box or manifold 26 has the advantage of the wafer residing on the grounded counter electrode or susceptor 16, which makes possible a high degree of plasma confinement that would not be achievable if the RF energy were applied to the wafer and the gas box were grounded. Additionally, the hardware is mechanically and electrically simpler since electrical isolation between wafer/susceptor and chamber is not required (or permitted). Temperature measurement and control of the susceptor/wafer in the presence of high frequency electric and magnetic fields is greatly simplified with the susceptor 16 grounded. Also, the feed-through 36 is rigid, eliminating flexible gas connections and the purge gas flow path safely carries any leaking process gas

into the chamber to the chamber exhaust. The capability to apply RF power to the gas manifold is made possible (despite the inherent tendency of high potential RF operation to form a deposition plasma within the feed-through) by the unique design of the feed-through, which drops the RF potential evenly along the length of the feed-through, thus preventing a plasma discharge within.

B. Wafer Transport System 18

As mentioned, this system is designed to transfer individual wafers 15 between the external blade, FIG. 2, and the susceptor 16 and to position the susceptor 16 and wafer 15 for processing. Referring further to FIG. 1, the wafer transport system 18 comprises a plurality of radially-extending wafer-support fingers 20 which are aligned with and spaced about the periphery of susceptor 16 and are mounted to a semi-circular mounting bar or bracket 38. Similarly, an array of radially-extending susceptor-support fingers 22 are spaced circumferentially about the susceptor 16, interdigitated with the wafer support fingers 20, and are mounted to a semi-circular bar 40 positioned just outside bar 38. The arcuate mounting bars 38 and 40 are mounted within a generally semi-circular groove 42 formed in the housing, and are actuated respectively, by vertically movable elevator assemblies 44 and 46.

As shown in FIG. 3, the susceptor elevator mechanism 44 includes a vertically movable shaft 48 that mounts the bar 38 at the upper end thereof. The shaft can be moved vertically up and down by various moving means 56, including a pneumatic cylinder, or, preferably, a stepper motor operating via suitable gear drive. Wafer elevator mechanism 46 is similar to the elevator 44.

The operation of the wafer transport system 18 is summarized by the sequence depicted schematically in FIGS. 4-8. In FIG. 4, the external blade 24 (with the wafer 15 to be processed supported thereon) is inserted via opening 56 into chamber 13 to a position over the susceptor 16. One example of a suitable blade 24 and associated robot wafer handling system (and door 25, FIG. 6) is described in EP-A-0272341. In this starting position, the wafer fingers 20-20 are positioned between the susceptor 16 and the blade 24.

Next, as shown in FIG. 5, the wafer elevator mechanism 44 raises the wafer-support fingers 20-20 above the blade 24 to pick up the wafer 15. The blade 24 is then withdrawn from the chamber 13.

As shown in FIG. 6, after retraction of the blade 24, a pneumatic cylinder closes door 25 over the blade access slot 56 to seal chamber 13. The susceptor elevator mechanism 46 is actuated to raise the susceptor-support fingers 22 and suscep-

tor 16 so that the susceptor 16 lifts the wafer 15 from the fingers 20-20 into position for processing in the area 14 immediately adjacent the gas distribution manifold 26. The spacing, d, between the wafer 15 and manifold 26 is readily selected by adjusting the travel of the elevator 46. At the same time, the susceptor fingers 22 and elevator mounting 46 maintains the horizontal orientation of the susceptor 16 and wafer 15 and parallelism between the wafer 15 and manifold 26 independent of the spacing, d.

After processing, and referring to FIG. 7, the susceptor elevator mechanism 46 lowers the susceptor fingers 22 and the susceptor 16 to deposit the wafer 15 on the wafer support fingers 20-20. The door 25 is then opened and blade 24 is again inserted into the chamber 13. Next, as shown in FIG. 8, elevator mechanism 44 lowers the wafer-support fingers 20-20 to deposit the wafer 15 on the blade 24. After the downwardly moving fingers 20-20 clear the blade 24, the blade is retracted, leaving the fingers 20 and 22 in the position shown in FIG. 4 preparatory to another wafer insertion, processing and withdrawal cycle.

C. Near-IR Radiant Heating System 30

The radiant heating system shown in FIGS. 2 and 9 provides a reliable, efficient and inexpensive means for heating the circular susceptor 16 and wafer 15 (e.g., silicon) in a manner that provides uniform wafer temperature, accurate absolute wafer temperature and rapid thermal response at low temperatures, preferably $\leq$ 600°C. In achieving these objectives, a number of requirements must be met. First, achieving uniform wafer temperature requires compensating the radiation losses at the edge of the wafer. Secondly, high efficiency at low wafer temperatures ($\leq$ 600°C) requires a high emissivity, high thermal conductivity susceptor 16 because silicon wafers have low emissivity at low temperatures in the near-infrared spectrum. In addition, near-infrared radiation is used to obtain fast heating response and for transmission through the inexpensive materials such as quartz window 70. The circular thin susceptor 16 has low thermal capacitance for fast heating and cooling response. These and the other objectives discussed below are achieved by the radiation heating system 30 shown in FIGS. 2 and 9.

The heating system 30 preferably comprises an annular array of small, inexpensive, single-ended vertically oriented lamps 58-58 which provide radiation in the near-infrared portion of the electromagnetic spectrum. The lamps 58-58 are mounted within an annular circular reflector module 60, preferably of aluminum. The module base 60 is formed from a block of aluminum, and has a pol-

ished annular reflecting channel 62 machined therein. The channel 62 has an arcuate, generally semi-circular reflecting base 64. The module 60 and lamps 58-58 are cooled by an annular cooling passage 66 that is formed within the collimating annular reflector 62. Connections are provided for the inlet and outlet of cooling liquid which, typically, is chilled water from a pressurized supply. Power is supplied to the lamp sockets 63 and associated lamps 58 by an electrical supply cable 68, typically from a variable power supply which automatically varies the lamp power based upon a predetermined program setting that is adapted to the requirements of the particular deposition process.

The annularly-collimated light from the vertical oriented lamps 58-58 is admitted into the chamber via a quartz window 70. Quartz is transparent to near-IR radiation. The transparent quartz window 70 is mounted to the housing 13 at the bottom of the process chamber 13 using annular seals 72-72 to provide a vacuum-tight interface between the window 70 and the housing. This mounting arrangement positions the radiant energy heating source 30 outside the chamber 13 at atmospheric pressure and isolates the vacuum of the processing chamber and the particulate-sensitive processing therein from the lamps. A bracket 74 can be joined to the lamp mounting base 60 and pivotally mounted by pivot pin 76 to a mating bracket 78, which is joined to the housing 12. (Alternatively, the lamp module can be bolted in place.) As a consequence of this pivotal mounting of the lamp assembly 30 external to and isolated from the process chamber 13, the lamp assembly is readily accessible for maintenance, lamp replacement, etc., by simply disengaging a clamp 79 to allow the assembly to pivot downwardly about pin 76.

As mentioned, the lamps 58-58 are small single-ended commercially available quartz-tungsten-halogen lamps which provide the required near-infrared radiation. One suitable lamp is the Ansi type "FEL" supplied by Sylvania, G.E., Ushio or Phillips. Presently, fourteen 500-1000W quartz-tungsten-halogen lamps that provide a wavelength of about 0.9 to 1.5 μm provide an annularly-collimated power density of up to about 94 W/cm² at the top of the lamp module. The maximum power density at the susceptor (substantially directed to the outer ~0.038m (1.5 in.) radius of a 0.142m (6 in.) diameter susceptor) is 2 17 W/cm² taking all efficiency into account (~ 15-16% efficiency). More generally, lamps concentrating their radiation in the range of about 0.7 to 2.5 μm wavelength would be particularly useful. The aluminum base 60 and concave-bottom, annular groove 62 provide a high collection-efficiency collimating reflector which directs a higher radiation power density at the

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susceptor edge than at the middle. This non-uniform, concentrated radiation heats the susceptor wafer circumferentially, which compensates the wafer edge heat losses and, thus, provides uniform wafer temperature over a wide range of chamber gas pressures and wafer temperatures.

In short, the desired uniform radiant wafer heating is provided by small, inexpensive lamps mounted in a compact simple aluminum module 60 that is easily cooled and maintained at a low temperature, and does not require plating. In addition, the use of the near-IR lamps and a thin, low mass, low thermal capacity, high emissivity susceptor of material such as graphite, provides maximum efficiency, fast thermal response, excellent temperature uniformity and transmission through the quartz window 70. Other susceptor materials include anodized aluminum, graphite coated with layers such as aluminum oxide (Al_2O_3), or silicon carbide, or a composite ceramic coated with Al_2O_3 or SiC or other materials. Also, interchangeable modules 60 having channels of different heights or diameters can be used to accommodate different susceptor and wafer diameters. A present version of the reactor is designed for 12.7 to 15.24 cm (5 to 6 in.) wafers. However, different lamp modules can be provided for smaller or larger diameter wafers by changing the module height and/or the radius of the module and the filament circle. Finally, the heating system 30 may employ a controller (not shown) such as a closed loop temperature control system using phase angle power control to provide rapid thermal response and rapid wafer temperature stability.

It should be noted that the simplicity, low mass and high performance characteristics of the heating system 30 are in contrast to prior wafer heating approaches which typically use a rectangular array of double-ended quartz-tungsten-halogen lamps. Conventional radiation heating practice has been to use a more massive susceptor and, if excellent temperature uniformity is required, to merely block radiation from the wafer center, thus sacrificing efficiency, rather than redirecting radiation. The advantages of the radiant heating system 30 over the conventional practices include in addition to the aforementioned uniform wafer temperature and much faster response time (both heating and cooling), smaller, less bulky more easily maintained equipment of higher reliability (long lamp lifetime); more efficient operation; and lower cost.

The use of the easily accessible, external radiant heat source 30 is facilitated and maintained by a gas purge system. As described in the succeeding section, this system directs purge gas flow across the vacuum side of the quartz window 70 to prevent deposition on the window and keep the window clean. Thus, the purge is a major contributor to lamp efficiency. This increases the number of process cycles between cleaning and, as a result, decreases the associated system downtime required for cleaning.

D. Gas Manifold 26 and Associated Distribution System

The gas distribution system 32 is structured to provide a unique combination of at least four structural features. First, the gas manifold 26 is one-half (the powered half) of an electrode pair. The powered manifold 26 provides high power. Second, the gas manifold 26 and other gas distribution surfaces are temperature controlled, which contributes to uniform deposition on the wafer 15 and prevents gas decomposition, deposition or condensation within the gas distribution system upstream from the plasma processing area 14 despite the use of reactant gases such as TEOS which condenses at ~ 35°C and decomposes or reacts with ozone at ~ 75°C. The external manifold temperature is controlled, e.g., to >100°C, to prevent the deposition of flaky, particulate-causing deposits. Third, the gas manifold 26 and gas distribution system 32 provide a clean, uniform deposition process. Fourth, the incorporated circumferential purging gas flow prevents deposition outside of the gas distribution area, i.e., outside the wafer on the internal chamber surfaces and gas distribution system surfaces.

The above features of gas distribution system 32 are depicted most clearly in the FIG. 2 vertical section view and the FIG. 10 enlarged vertical section view. The gas manifold 26 and associated distribution system are part of the housing cover 80, which is pivotably mounted to the housing 12 by pivot means (not shown) to facilitate access to the interior of the housing, including chamber 13, plasma process chamber 14, and associated internal components of the wafer and susceptor elevator mechanisms (44,46).

The process gas flow from the feed-through 36 is directed into the cover 80 by inlet bore 88 which communicates with, that is, feeds into, gas manifold chamber 90 formed by the apertured manifold face plate 92. A uniquely designed baffle plate 94 is mounted within the gas manifold chamber 90 by means such as standoffs (not shown) to route the process gas around the outside of the edge of the baffle 94 and then radially inwardly along the bottom of the baffle and out the apertures 96-96 in the manifold plate into the plasma processing region 14 above wafer 15.

The cover 80, including the manifold 26 thereof, is heated (or cooled) by an internal flow of fluid or liquid such as de-ionized water along internal path 81 defined by inlet channel 82, annular channel 84 and outlet channel 86. Preferably, this flow

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keeps the face plate 92 within the range 100°C - 200°C, in order to ensure that any deposition on the face of the gas manifold which is exposed to the plasma is a hard film. A poor film formed on this surface can create particulates and this must be avoided. Also, the flow preferably holds baffle 94 within the range, most preferably within 35°C-65°C, to prevent internal deposition or condensation of low vapor pressure process gases such as TEOS and to prevent decomposition and reactions of gases such as TEOS and ozone. Please note, such deposition is directly proportional to time, temperature (t,T). Thus, the very small gap "d" of about 2.54×10^{-3}-5.08×10^{-3}m (0.1 to 0.2 inches) between the plates 94 and 92 also decreases any tendency to internal deposition.

As an example, in one process application involving the deposition of silicon dioxide, oxygen, TEOS and a carrier gas are inlet from manifold 26 to the chamber 14 at chamber pressure of 66.7-26664.4Pa (0.5-200 torr) to form a reactant species for deposition. Wafer 15 is heated to 375°C, and hot de-ionized water (water temperature 40°C to 65°C) is inlet along path 81 at an adequate flow to keep plate 92 at < 65°C, to prevent condensation of the TEOS, and to keep plate 94 >100°C. (De-ionized water is used because the manifold 26 is the RF powered cathode and de-ionized water is a non-conductor.) More generally, the inlet temperature of the water is selected as required for a particular deposition process and its associated gas chemistry and/or other parameters in order to maintain both the internal surfaces and the external surfaces of the gas box 90 at desired temperatures.

To reiterate, the process gas flow is along path 91 defined through inlet bore 88, into manifold chamber 90, radially outwardly to the edge of baffle 94 and around the baffle periphery to the bottom thereof, then radially inwardly between the baffle 94 and the manifold plate 96 and out holes 96-96 into the plasma processing region 14 above the wafer 15. The flow path of the deposition gas emerging from holes 96-96 is generally radially outwardly across the wafer.

In addition, the small volume of the vacuum process chamber 14 and the high useful chamber pressure range of about 66.7 Pa (0.5 torr) to near-atmospheric pressure also contribute to the tendency to provide a uniform flow radially outward from the center of the wafer 15 with uniform deposition on the wafer and purging without deposition other than on the wafer.

The manifold holes 96-96 are designed to promote this uniformity of deposition. The holes (as well as the manifold temperature, discussed above) are also designed to avoid the formation of deposits on the manifold outer (bottom) surface 97 and,

in particular, to prevent the deposition of soft deposits on surface 97 which could flake off and drop onto the wafer during and after processing. Briefly, the hole array is one of generally concentric rings of holes 96-96. The distances between adjacent rings (ring-to-ring spacings) are approximately equal, and the hole-to-hole spacing within each ring is approximately equal. However, the patterns are angularly staggered so that no more than two adjacent holes (or some other selected number) are aligned radially. That is, the holes in the gas distribution plate 92 are equally spaced on circles so the hole locations do not form radial straight lines, thereby substantially decreasing deposition on the gas distribution plate itself and enabling uniform gas flow and deposition on the wafer.

The hole length through the manifold 92, i.e., the thickness of the manifold plate 92, and the transverse hole diameter are also selected to promote uniform deposition. Increasing/decreasing the hole length has the effect of decreasing the deposition thickness inside-out/outside-in, as does increasing/decreasing the hole diameter.

In a presently used configuration, approximately 3400 holes 96-96 are used. The hole length is 2.54×10^{-3}-3.81×10^{-3}m(0.100 to 0.150 in), the hole diameter is 0.71×10^{-3}-0.89×10^{-3}m(0.028 to 0.035 in.) and the radially asymmetric holes are located on approximately 2.20×10^{-3}m(0.090 in.) centers. These dimensions and the associated configuration provide a uniform flow pattern and substantially decrease deposition on the manifold plate 92. The present ~ 0.152m (6 in.) manifold diameter will accommodate wafer diameters as large as ~ 0.152m (6 in.) Larger wafers can be processed by changing to a larger manifold 26, susceptor 16, larger diameter suspector 16 and wafer support finger arrays, and by altering the lamp module 30 as described previously.

Referring further to FIG. 10, as indicated by the arrows 93, 95, 97 a first, upper purge gas flow path is provided in cover 80 and manifold 26. That is, purge gas flow from the RF/gas feed-through 36 is routed into inlet bore 98 in cover 80 (arrow 93) which feeds into radial channels or grooves 100 that in turn feed into an annular groove 102 formed in the cover concentric with and just above and outside the manifold chamber 90 (arrow 95). A ring flow turner 104 is mounted concentrically within manifold plate rim 105 and forms a peripheral channel 106 at the inside of the manifold rim that connects the annular channel 102 to the three outer rows of apertures 108 in the manifold plate 92.

As shown in FIG. 11, the purge holes 108-108 are arranged similarly to the process gas holes 106-106 in generally concentric rings that are spaced at approximately equal ring-to-ring distances. The within-ring hole spacing is selected so

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that the locations of the purge holes 108-108 form staggered radial lines, i.e., so that no two adjacent purge holes are along a radial line. For the above-described exemplary manifold, the gas is distributed from about 600 holes and the following purge hole dimensions are used: between-ring spacing 2.29×10^{-3}m (0.090 in.); hole diameter 0.64×10^{-3}m (0.025 in.); and hole length 1.02×10^{-3}m (0.040 in.)

Referring to FIG. 2, a second, lower purge flow path 101, 103, 105 is provided via inlet bore 110, formed in the side of the housing 12, which connects or feeds into an annular channel 112 formed generally concentrically about the lower section of the process chamber 13 just above the quartz window 70. The channel 112 has holes that are spaced about the lower region of the chamber 13 or· equivalent yielding feature to feed the lower purge gas uniformly across the quartz window 70 (see arrows 103), around the lower edge of the wafer 15 (arrows 105) and across horizontal quartz cover plate 114, which surrounds the chamber 13 just below the wafer processing chamber 14. Referring also to FIG. 1, the plate 114 contains an annular pattern of holes 116 therein which are aligned with an annular gas outlet channel 118. This channel is connected via outlet bore 121 to a conventional vacuum pumping system (not shown), which establishes the vacuum within the chamber and exhausts the spent gases and entrained gas products from the chamber.

As mentioned (see FIG. 10), the upper purge gas flow is through inlet 98 (arrow 93), channels 100, 102 and 106 (arrow 95), then out purge ring apertures 108-108 (arrow 93) at the outer upper edge of the process-positioned wafer 15. Simultaneously (see FIG. 2), the lower purge gas flow is through inlet 110 (arrow 101) and annular ring 112 across the quartz window 70, sweeping the window clean (arrow 103), then upwardly toward the lower peripheral bottom edge of the wafer 15 (arrow 105). Referring to FIG. 10, the upper and lower gas purge flows 97 and 105 merge at the wafer's edge and flow outwardly as indicated by arrow 107 across the plate 114 and through the holes 116 therein into the annular exhaust channel 118 and out of the chamber along path 109 (FIG. 2). This upper and lower, merging flow pattern not only keeps the quartz window 70 clean, but also sweeps spent deposition gases, entrained particulates, etc., out of the chamber 13. The combination of the dual, upper and lower purge flows which are conformed to the inner quartz window chamber surfaces and to the circumferential wafer edge and the very high chamber pressures (unusually high for PECVD) provide a very effective purge and prevent deposition external to the wafer.

Equally important, uniform radial gas flow is provided across the wafer 15 by the multiplicity of holes 116-116, illustratively five in number, which are formed in the distributor plate 114 peripherally around the wafer 15. These holes 116 communicate into the larger semi-circular exhaust channel 118 which, in turn, is connected to the vacuum exhaust pumping system via the single outlet connection 121. The channel 118 has large conductance relative to the holes 116-116 because of its relatively very large volume, which provides uniform pumping at all points radially from the wafer, with the simplicity of a single point pump connection. In combination with the uniform gas flow distribution inlet pattern provided by manifold 26, this uniform radial pumping provides uniform gas flow across the wafer 15 at all pressures and, thus, uniform deposition even at very high chamber pressures such as 26664.4 Pa (200 torr) and above.

Also, the manifold 26 is usable as an electrode for a uniform glow discharge plasma at unusually high pressures, which enables both the very high deposition rate and the effective purge flow.

E. Anti-Electrical Breakdown Gas Feed-Through 36

As mentioned, the advantages of using the gas box 26 as the powered RF electrode include the wafer residing on the grounded counter electrode, which makes possible a high degree of plasma confinement that would not be achievable if the RF energy was applied to the wafer and the gas box was grounded. Additionally, the hardware is mechanically and electrically simpler since electrical isolation between wafer/susceptor and chamber is not required (or permitted). Temperature measurement and control of the susceptor/wafer in the presence of high frequency electric and magnetic fields is greatly simplified with the susceptor grounded.

However, applying high power, high frequency, large potential RF energy to a conventional gas distribution system and, in particular, across a short distance between metallic gas tubing and gas manifold normally would cause premature electrical breakdown of the process gas within the distribution system upstream of the plasma processing chamber. In other words, in conventional systems the RF voltage would create a plasma within the distribution system, which would cause unwanted deposition of the process gas on the internal surfaces of the gas distribution system.

Our combination RF/gas feed-through 36 (FIG. 12) is designed to apply RF power to the gas box 26, that is, to use the gas box as the powered RF electrode, without breakdown of the process gas and without deposition within the gas distribution system.

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Also, consistent with one of the overall objectives of achieving a small, compact CVD reactor, the RF/gas feed-through 36 is of a compact, low profile design, despite our design objective that the high RF potential be applied parallel to the gas flow path to yield a constant voltage gradient over a distance to eliminate the high local electric field which causes electrical breakdown.

It should be mentioned that prior gas feed-throughs are incapable of achieving the above objectives. Two such prior art approaches are known to us. The first approach flows the gas within an insulating tube between surfaces that are at a high electric potential difference. A second approach flows the process gas through an insulator between the surfaces of high electric potential difference at sufficiently high gas pressure so that electrical breakdown does not occur. The first approach is not compact and does not work at high frequencies, where electrical breakdown is more efficient (see, e.g., curve 201 and 200, FIG. 14). Also, this first approach is not capable of operation where there is a small p•d (pressure•distance) product. The second approach is more compact than the first, and less susceptible to electrical breakdown at high frequencies, but is also subject to electrical breakdown where there is a small pressure•distance product.

Referring now to FIG. 2 and, primarily, to FIG. 12, the feed-through 36 comprises an inlet end connector or manifold 120, an outlet end connector or manifold 122 and an intermediate gas feed structure 124 comprising a quartz tube 126 and an elongated insulating transition housing 128. The block 128 is mounted to and between the end connectors 120 and 122 using O-ring seals 130-130 to provide vacuum-tight mounting. The internal bore 127 of the quartz tube 126 communicates with gas inlet bore 134 in the inlet end connector and gas outlet bore 136 in the outlet end connector.

Process gases and purge gas under pressure from sources such as an ozone generator, a liquid-TEOS vaporizer, and conventional pressurized gas tanks or bottles are routed through conventional valves or an automatic flow control system for controlled flow rate application to the inlet manifold 120.

As indicated by arrows 131-135, process gas is routed through the feed-through device 36 via the inlet bore 134 and through the quartz tube 126 and out the outlet bore 136 and into the mating inlet bore 88 in the gas distribution head 32. Please note, the feed-through is shown enlarged in FIG. 12 to facilitate illustration. The actual feed-through 36 is of a size so that the gas outlets 136 and 146 are aligned with the mating channels or bores 88 and 98 in the reactor cover 80.

The purge gases are routed through the feed-through co-axially with the process gas flow path so that if there is a leak along the process gas path 131-133-135, the process gas is harmlessly transported into the process chamber 14 along with the purge gas and, thus, does not escape into the ambient.

The incoming purge gas is applied to inlet bore 138 in the inlet end connector 120. Bore 138 communicates with an annular channel 139 formed in the spool-shaped fitting 140 which is mounted near the inlet end of the quartz tube 126. This spool fitting 140 is sealed at the outer end thereof by cylindrical flange fitting 142 and O-ring seal 144. The annular channel 139 communicates via holes (not shown) with the annular passage 147 between the tube 126 and concentric block 128. The passageway 147 feeds similarly into annular chamber 139 in fitting 140 at the outlet end of the tube 126. The tube 126 is mounted and sealed at the outlet in the same way described above relative to its inlet end. At the outlet end, chamber 139 feeds into the outlet bore 136. This arrangement provides an isolated purge gas flow path through the feed-through 36, as indicated by arrows 148-156.

The co-axial gas feed apparatus described above provides a dual barrier which prevents the leakage of potentially toxic process gases into the atmosphere. That is, the path to the ambient between mating surfaces is barred by the two sets of O-ring seals 130 and 144. These seals are positioned in series along the potential path to the ambient. Also, as mentioned, in the event of internal system leaks such as a leak in the quartz tube 126, the purge gas flow carries the process gas into the process chamber 14, where both are exhausted by the chamber vacuum system. In addition, the process and purge gases are routed entirely through the chamber components, i.e., through substantial blocks/bodies such as the aluminum connectors 120 and 122 and the insulator block 128. Consequently, external, typically flexible, gas tubing is eliminated at the reactor. The very solid, secure routing fixtures, the dual seal barriers, and the co-axial gas flow in which the purge gas flow surrounds the process gas flow, provide a safe, secure process gas flow path in the reactor and feed-through device.

As shown in FIG. 12, the inlet end connector 120 is connected to ground. The outlet end connector 122 is connected to the RF power supply 128 and connects the RF energy to the cover 80 and manifold plate 92. A constant electric potential gradient is provided along the column of process gas flow between the grounded connector 120 and the driven connector 122 by providing one of three types of constant voltage gradient elements along the surface of the quartz insulating tube 126: a

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radio frequency coil which provides resistive, inductive, or capacitive (effective) impedance; a resistive film; or a resistive sleeve.

As shown schematically in FIG. 13A, the RF coil 160 is a wire coil that is wound around the quartz gas tube 126 between the ends thereof and the high voltage which is applied across the tube length. Preferably, the wire coil 160 is of No. 24 to No. 26 AWG aluminum wire. The desired electrical impedance at the frequency of operation is obtained by selecting the wire material, diameter, number of turns per unit length, length and the winding technique. This A.C. impedance can be selected to have a net inductive/resistive impedance or a net capacitive/resistive impedance or to be purely resistive (resonant). The A.C. and D.C. resistance can be selected (using wire diameter, length, and material). A typical application has a high inductive reactance but is a D.C. short. For a radio frequency driven system of 13.56 MHz, typical values for the inductance of an RF coil-type feed-through are approximately 10×10^{-6} to 15×10^{-6} Henries. For the resistive film or sleeve feed-through, a resistance of 100×10^3 to 500×10^3 ohms is typical.

Alternatively, as shown in FIG. 13B, a resistive film 162 of material of controlled electrical resistivity and thickness, such as Acheson "Aerodag G" (a colloidal suspension of micron size graphite particles in an isopropyl alcohol dispersing medium), is coated on the outside of the quartz tube 126 to provide the desired resistive impedance and allow broad band (frequency) operation.

The third alternative shown in FIG. 13C uses a solid resistive sleeve 164 of a material such as a composite ceramic of controlled electrical resistivity, to provide the desired electrical resistive impedance and broad band frequency operation.

Still another alternative, a variant of the solid resistive sleeve 164, uses a sleeve of material which is ferromagnetic with very high permeability at the frequency of interest, and has controlled electrical resistivity. Operation is the same as for the resistive sleeve 164, with this added advantage. Should breakdown occur under severe conditions, the presence of magnetic material and initially high current and resulting high magnetic field produces a very large inductive reactance to charge flux (current), which very quickly reduces then extinguishes electrical conduction in the process gas.

FIG. 14 illustrates representative bench test data for a quartz tube without a constant voltage gradient device of voltage breakdown in kilovolts as a function of pressure in torr at both low (100×10^3Hz) and high (13.56×10^6Hz) radio frequencies. As indicated, for the pressure range of 666.7-2666.4 Pa (5-20 torr,) the breakdown range was 3 to 7000 V for the low radio frequency and approxi-

mately 2000-5000 V for the high radio frequency.

FIG. 15 illustrates bench test data of breakdown voltage as a function of pressure for Tube A, a tube of length 0.105m and diameter 0.006m without a constant voltage gradient device, and Tube B, the same tube with a constant voltage gradient device of the wire coil type, 160, consisting of 160 turns of ±26 AWG wire. Tube C was the same as tube B, except for having a greater length, 0.134m. - This illustrates that the RF/gas feed-through 36 is very effective in preventing breakdown and subsequent deposition of process gases under actual reactor operating conditions. In fact, typically the reactor system 10 will be used at pressures of up to 26664.4 Pa (200 torr) and above, at which values the breakdown voltages will be much higher than those depicted in FIG. 14.

In short, the anti-electrical breakdown gas feed-through 36 of the present invention provides a constant voltage gradient along the process gas flow column, without charge build-up. In addition, the feed-through 36 is designed to incorporate resistive, inductive or capacitive electrical impedance between the high potential difference ground and driven surfaces. The choice of impedance depends upon the electrical requirements of the system, i.e., low frequency, high frequency, wide band, d.c. operation, etc. This constant electrical potential gradient effectively prevents premature breakdown and deposition within the gas distribution system 32 and feed-through 36 at high or low radio frequencies. In addition, the structure of the feed-through 36 including the coaxial gas feed (the purge gas flow outside the quartz tube and the process gas flow inside the quartz tube) is highly resistant to process gas leaks and purges any process gas leaks into the system exhaust.

Finally, it should be mentioned that temperature controlled water can be flowed through channels (not shown) in the feed-through device 36 isolated from process and purge channels to (heat or cool) control the temperature of the gas in the feed-through. In a typical application which uses gases such as ozone or TEOS, it is important that the gas temperature be controlled so that, for example, condensation (feed-through too cold), decomposition (too hot), or chemical reaction (too hot) do not occur within the tube. Any of the above occurring inside the gas feed-through device could severely affect the desired process. Additionally, if the gases reacted inside the quartz tube, deposition could occur inside the tube.

F. Summary of Certain Key Features

1. Uniform Wafer Heating

Our reactor uses a tailored non-uniform near-IR radiant heating pattern and a thin, low mass high emissivity susceptor to provide thermal efficiency, fast thermal response (heating and cooling), excellent temperature uniformity despite the inherent non-uniform heat losses of thin circular wafers, and good transmission through a chamber window of quartz or the like (which permits external mounting of the radiant heating module).

2. Gas Distribution System

The RF powered gas manifold 26 provides the necessary high power to enable confinement of the plasma. Also, the uniform gas inlet flow pattern provided by the gas manifold and radial exhaust pumping provide uniform gas inlet and exhaust (purge) pumping and uniform radially gas flow across the wafer, enabling uniform processing (deposition/etching) over a wide pressure regime including very high pressures. The radial pumping and high pressure capability provide confinement of the plasma/reactant species to the wafer and, in enabling effective purging, prevent deposition within the chamber except on the wafer. The precisely temperature-controlled internal and external surfaces of the gas manifold prevent decomposition, reactions, condensation, etc., within the gas box and eliminate undesirable particulate-generating deposits on the external gas box surfaces. For example, temperature controlled water is circulated within the gas box to maintain the temperature between about 35°C-75°C to prevent internal deposition or condensation of TEOS below about 35°C and to prevent internal decomposition of or reaction between ozone and TEOS above about 70°C, and to maintain the external face of the gas manifold greater than about 100°C to prevent flaky external deposits.

3. Gas Feed-Through

The gas feed-through provides the enables the application of high voltage RF power to the gas box, as well as the application of purge gas and process gas to the gas box, without gas breakdown.

4. Wafer Transport System

A one-axis robot susceptor/wafer support and transport system is adapted to load and unload wafers at a selected position within the chamber onto and from an external robot blade. This trans-port system provides variable parallel close-spacing between the susceptor/wafer and the overlying gas manifold and provides variable spacing by simply selecting the vertical travel of the associated susceptor support fingers and susceptor elevator mechanism. The parallelism increases plasma stability and uniformity by eliminating the tendency to run to one side or the other and, thus, enables uniform processing (deposition and etching). The variable close spacing of the distance, d, between the outer face of the gas manifold and the wafer surface facilitate the implementation of different types of process. Also, the spacing can be set at a very small variable dimension such as, for example, one centimeter, 0.5 centimeter and even smaller, to enable confinement of the plasma and/or gaseous reactants between the gas distributor and the wafer. This confinement increases the reaction efficiency and increases the rate of the reaction (deposition or etching) and helps prevent deposition everywhere except on the wafer, and even at very high chamber pressures.

5. Wide Pressure Range, High Pressure Regime

High pressure capability results from a number of the above-summarized factors including uniform radial pumping, the uniform gas flow provided by the gas manifold, the confinement provided by the variable close spacing between the electrodes and the application of high power density RF power to the gas manifold as discussed in greater detail below.

G. Relevance of Features to Multiple Process Capability

The above key features can be summarized as follows: (a) Wide pressure, high pressure regime; (b) Temperature uniformity of susceptor wafer; (c) Uniform flow distribution; (d) Variable close spacing of electrodes (inlet gas manifold and susceptor) with parallelism; and (e) Temperature control of internal/external gas inlet manifold surfaces.

Typically, at least several of these features are very important to each type of processing for which our reactor has been used. These key features are summarized below on a process-by-process basis.

1. Thermal Chemical Vapor Deposition

(a) Wide pressure, high pressure regime.
(b) Temperature uniformity of susceptor/wafer.
(c) Uniform flow distribution.
(d) Variable close spacing of electrodes.
(e) Temperature control of internal/external gas inlet manifold surfaces, especially where unstable gases such as TEOS and ozone are used.

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2. Plasma-Enhanced CVD

(a) Wide pressure, high pressure regime.
(c) Uniform flow distribution.
(d) Variable close spacing of electrodes with parallelism.
(e) Temperature control of internal/external gas inlet manifold surfaces.

Temperature control of the gas box external surface to >100°C is important to prevent the deposition of porous particulate causing films.

High pressure operation increases ion scattering, which decreases bombardment of and damage to the wafer and enhances step coverage. This, because high pressure operation dilutes the concentration of the gas molecules to the point where they do not react at a sufficient rate to cause particles/unwanted deposition on surfaces. The high pressure capability and associated decreased bombardment enables one to decrease the bombardment level for a given power/voltage and reaction rate or, alternatively, to use higher power/voltage to obtain a higher reaction rate for a given bombardment level. Uniform flow distribution is also critical, particularly at the close spacing of less than one centimeter used in our reactor, because it confines the plasma and thus enhances clean operation. The ability to adjust the electrode spacing with parallelism permits the use of the close spacing with the plasma stability necessary for deposition.

3. Plasma-Assisted Etchback

(a) Wide pressure, high pressure regime.
(d) Variable close spacing of electrodes.

The variable large spacing in combination with the high pressure capability permits effective etchback. The variable spacing between electrodes is very important because it would be impossible to optimize the etch and other processes without varying the electrode spacing used for deposition. For example, a typical spacing of <1 cm is used for thermal CVD and PECVD while the etchback requires a spacing of ≈0.4 in. or 1 cm.

4. Reactor Self Clean

(a) Wide pressure regime.
(b) Variable close spacing of electrodes (inlet gas manifold and susceptor) with parallelism.

The variable spacing in combination with variable pressure permits effective reactor self-cleaning. Here, the required spacing, d, ≈ 0.01m (0.4 in.) is larger than that required for, e.g., thermal CVD and PECVD. The relatively larger spacing and wide pressure regime permits the plasma to diffuse within the reactor (rather than being confined as re-

quired for the deposition processes) and clean the entire reactor. A typical self-cleaning sequence uses RF power of 500 W, gas NF_3 or other fluorine containing chemistry at flow rates typically of 1 x $10^{-2}m^3/min$ (0.1 slm) pressure of 66.7 PA (0.5 torr) and d ≈ 0.01m (0.4 in.), and has provided ebb rates of ≈ 0.5 μm/sum (0.5 micron/sum).

5. Sputtering Topography Modification

(a) Wide pressure, high pressure regime.
(b) Variable close spacing of electrodes (inlet gas manifold and susceptor) with parallelism.

Here, the high pressure capability combined with $5.08 \times 10^{-3}m$ (0.2 in.) spacing as well as the ability to apply RF power to the gas box at high power levels permits sputtering of materials such as oxide or other drelectrics using gas chemistry such as argon or other heavy molecule gas chemistry such as $SiCl_4$. A typical sputtering process involves application of RF power of 700 W gas flow rates 1 x $10^{-2}/min$ (0.1 slm), pressure of 10 mt. electrode spacing, d, of 5.08 x 10^{-3} to 12.7 x $10^{-3}m$ (0.2 in to 0.5 in.).

II. Multiple Step In-Situ Planarization Process and Steps

The processing steps and multiple step processing sequences described here were performed in the reactor 10. The ability to perform multiple step processing using temperature sensitive gases such as ozone and TEOS and different steps such as CVD, PECVD, etching, and self-cleaning in-situ qualifies the reactor 10 as being uniquely preferred. However, the process disclosure here will permit those of usual skill in the art to practice the process sequences albeit in single process, dedicated reactors and to adapt such reactors, e.g, to the use of the process.

A. Low Temperature Thermal CVD of Conformal SiO_2

The thermal chemical vapor deposition of highly conformal silicon dioxide is an improvement of methods which use the pyrolysis of TEOS and oxygen. The present thermal CVD invention is based in part upon the discovery that improved highly conformal (~100%) silicon dioxide coatings are formed by the thermal chemical vapor deposition of the reactants TEOS and ozone at relatively low temperatures, using lamp radiant heating to provide a wafer temperature of about 200°C - 500°C, and high pressures. The ozone lowers the activation energy of the reaction kinetics and forms silicon dioxide with the TEOS at the relatively low temperatures of about 200°C to 500°C. A com-

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mercially available high pressure, corona discharge ozone generator is used to supply a mixture of (4-8) weight percent ozone in oxygen to the gas distributor. Helium carrier gas is bubbled through liquid TEOS to vaporize the TEOS and supply the diluted gaseous TEOS in the He carrier to the gas distributor.

In particular, the thermal chemical vapor deposition process uses the reactants ozone (O_3), oxygen and tetraethylorthosilicate (TEOS) at a low temperature within the range of about 200°C-500°C and at a high pressure within the range of about 1333.2-26664.4 Pa (10-200 torr) and, preferably about 5332.9-15998.6 Pa (40-120 torr), to deposit a highly conformal silicon dioxide coating that fills in the voids, cusps and topographical irregularities and thereby provide a substantially planar surface. In the presently preferred embodiment, the ozone is applied at a flow rate of 2 x 10^{-3} to 3 x 10^{-3} m³/min. (2 to 3 slm), the helium carrier gas flow rate is 50 x 10^{-6} m³/min. to 1.5 x 10^{-3} m³/min. (50 sccm to 1.5 slm), the chamber pressure is 5332.9-15998.6 Pa (40 to 120 torr) and the wafer temperature is 375°C±20°C, thereby providing a highly conformal undoped silicon dioxide coating at a deposition rate of 5.0x10^{-9} m/s.

As mentioned, the gas distribution manifold (gas distributor 26) of the reactor 10 is controlled by de-ionized water of temperature 20-50°C circulating in passages therein to maintain the internal surface of the gas distributor 26 within the narrow range of about 35°C-75°C, i.e., at a temperature of less than about 75°C to prevent decomposition of the TEOS and reaction between the TEOS and ozone and above 35°C to prevent condensation of the TEOS inside the gas distributor.

The distance, d, from the temperature-controlled gas distributor to the surface of the substrate is preferably approximately one centimeter or less. This distance of one centimeter or less confines the plasma or gaseous reactants between the gas distribution 26 and the wafer 15. This increases the reaction efficiency, and increases the rate of the reaction (deposition) and helps to prevent deposition everywhere except on the wafer.

The thermal CVD process of the present invention uses unusually high deposition chamber pressures: pressures of preferably at least ≥ 1333.2 Pa (10 torr) and of about 2666.4 to 26664.4 Pa (20-200 torr) are utilized. Even the lower portion of this range is over 20 times greater than the total pressure normally utilized in processes utilizing TEOS. The high pressure increases the density of available reactive species and, thus, provides a high deposition rate.

Furthermore, the use of high pressure enables an effective purge. The high purge flow rate improves the ability to remove waste gases, entrained

particulates, etc., without unwanted deposition on the chamber surfaces. The above-described bottom purge flow sweeps radially outwardly across the bottom side of the susceptor wafer. The bottom flow is joined by an upper purge flow that is directed downwardly at the wafer's periphery. The combined streams flow radially outwardly from the periphery of the wafer, and cause the deposition gas to flow radially uniformly outwardly, then through the exhaust system of the chamber at very high flow rates. For example, useful top purge gas flow rate (preferably nitrogen) may be from 1 x 10^{-3} to 10 x 10^{-3} m³/min. (1 slm to 10 slm) and the bottom purge gas flow rate (again, nitrogen) may be 1 x 10^{-3} m³/min. to 20 x 10^{-3} m³/min. (1 slm to 20 slm). These high pressure, high flow rate top and bottom flows purge unwanted gases and particulates everywhere without disrupting the uniform deposition gas distribution at the top of the wafer.

Using the reactor 10, the presently contemplated useful flow rate range of the helium gas (the carrier for (TEOS) is 1.67x10^{-6} to 83.3x10^{-6} m³/s (100 sccm to 5 slm) (sccm = standard cubic centimeter per minute; slm = standard liters per minute) and the associated ozone, O_3, flow is provided by the composition of 4 to 8 weight percent ozone in oxygen flowing at a rate of about 1.67x10^{-6} to 166.7x10^{-6} m³/s (100 sccm to 10 slm). The total gas flow rate, not including the purge gases, typically can be within the range 3.33x10^{-6} to 250.0x10^{-6} m³/s (200 scan to 15 slm).

The above-described gas flow, chamber pressure, and resulting chamber temperature have provided a silicon dioxide deposition rate of about 0.83x10^{-9} m/s to 6.67x10^{-9} m/s (500 Angstroms/min. to 4,000 Angstroms/min.).

While useful deposition rates of 0.83x10^{-9} and 0.67x10^{-9} m/s (500 and 400 Angstroms/min) have been achieved at corresponding temperatures of 200°C and 500°C, as shown in FIG. 20 the deposition rate peaks at about 375°C ± 20°C. The decreased deposition above and below the peak is a consequence of unfavorable reaction kinetics at the surface of the substrate. Fortuitously, the peak temperature is also close to the maximum processing temperature of about 400°C for aluminum-containing multiple conductor structures. Above ~ 400°C, hillocks form in aluminum. Above ~ 500°C, aluminum softens.

Referring to FIG. 21, using an (ozone and oxygen):helium flow rate ratio of 2:1 33.3x10^{-6} m³/s (2 slm) of 8 wt. percent ozone in oxygen: 16.7 m³/s (1 slm) He carrier and TEOS the deposition rate saturates at 5x10^{-9} m/s (3,000 Angstroms/min) at a chamber pressure of 10665.8Pa (80 torr), and wafer surface temperature of 375°C (using a TEOS temperature of 35°C), with very little increase at

higher pressures. Decreasing the temperature to 200-375°C at 10665.8 Pa (80 torr) decreases the deposition rate to 1.67×10^{-9} to 5.00×10^{-6} m/s (1,000-3,000 Anstroms/min), respectively. At 2666.4 Pa (20 torr), temperatures of 200-375°C provide a deposition rate of 0.83×10^{-9} to 1.67×10^{-9} m/s (500-1000 Angstroms/min). Above pressures of about 15998.6Pa (120 torr), gas phase reactions increase particulates. This can be controlled by decreasing the wafer temperature or increasing the diluent flow rate, but these steps decrease the deposition rate.

While the resulting films have been characterized as having improved physical and electrical properties such as cracking resistance, density, refractive index, shrinkage, rate of etching, breakdown voltage, flat band voltage, mobile ion contamination, pin hole density and silicon oxide purities, the crucial aspect is the excellent ~100% conformal coverage over vertical and horizontal surfaces of steps and over other surface irregularities. Consequently, problems such as overhang, cusps and voids are much less severe, thereby minimizing or even eliminating the amount of follow-up processing which must be done to remedy such problems and to achieve planarization.

Furthermore, this high conformality coverage is provided using underlined undoped oxide coatings. Conventional processes use reflowing to smooth the deposited oxide and incorporate phosphorus or boron doping (phosphosilicate glass, PSG, borosilicate glass, BSG, and borophosphosilicate glass, BPSG) to lower the reflow temperature. Our thermal CVD process eliminates the need for reflowing and, thus, the use of PSG, BSG and BPSG and associated problems such as aluminum corrosion. However, if desired, in our thermal CVD process, the conformal oxide could be doped to a low level of, e.g., 1 weight percent to 10 weight percent of phosphorus and/or boron by incorporating reactants such as TMP (tetramethylphosphite) and/or TMB (tetramethylborate). The low concentration doping level would provide sufficient reflow characteristics.

B. Two-Step Planarization Process

In one aspect, the process of the present invention is an improvement of conventional methods for planarizing silicon dioxides such as, for example, conventional methods using spin-on glass and polyimide deposition with etch-back.

Another aspect of the present invention is the use of the above-described thermal CVD silicon dioxide deposition process to substantially planarize a dielectric layer, followed by the use of an isotropic wet or dry etch, preferably at a high etch rate, to complete the planarization process. The combination of the above-described low temperature, thermal CVD, conformal oxide deposition process in conjunction with various wet or dry isotropic etch steps provides an unexpectedly conformal, planarized dielectric layer which serves well in the small geometry, multi-level metallization structures that are currently being developed and will be developed in the future. Described below is a presently preferred dry isotropic etch process which can be performed in-situ, in the same, referenced multi-step chamber.

C. Three-Step Planarization Process

In another aspect the present invention is embodied in a three-step process which, first, forms a layer of silicon dioxide, preferably at a high deposition rate; the above-described ozone and TEOS-based thermal CVD conformal oxide deposition process is used as the second step to form a highly conformal oxide coating; then, in the third step, a preferably high rate isotropic etch is applied to quickly complete the planarization process.

D. Preferred Three-Step Planarization Process

In another aspect of the present invention, the above-described thermal CVD, conformal oxide deposition process is used in a three-step high deposition rate, high throughput planarization process in-situ in the referenced multiple process CVD/PECVD deposition chamber. The planarization process can be applied over existing dielectric layers or can be used alone to form a planar dielectric.

The preferred first step is a PECVD oxide deposition. The PECVD oxide deposition process uses a plasma formed from TEOS, oxygen, and a carrier gas with or without a diluent such as helium. This process uses a deposition chamber pressure of from about 133.3Pa to about 6666.1Pa (1 torr to about 50 torr); an oxygen flow rate of from about 1.67×10^{-6} to 16.7×10^{-6} m³/s (100 sccm to 1,000 sccm), an inert carrier gas (helium) flow rate of from 1.67×10^{-6} to 25.0×10^{-6} m³/s (100 to 1,500 sccm), a total gas flow rate (not including the purge gases) of 3.33×10^{-6} to 41.7×10^{-6} m³/s (200 sccm to 2.5 liters per minute), and RF power to the ~ 0.15m (6 in) diameter gas distributor cathode of about 200 - 400 watts. Power density at the gas distributor/cathode 26 is about 10×10^3 W/m² (1 watt/cm²) based on calculations for a quasi-parallel plate configuration. Radiant energy is directed to the susceptor from below by the annular array of vertical lamps to generate a deposition plasma and heat the wafer surface to a temperature of 300 to 500°C. Top (nitrogen plus helium mixture) and bottom (nitrogen only) purge gas glow rates of 1×10^{-3} to 15×10^{-3} m³/min. (1 to 15 slm) and 1×10^{-3} to 20×10^{-3} m³/min. (1 to 20 slm) respec-

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tively, are used with respective preferred top and bottom purge gas flow rates of 2.5 x 10^{-3} to 10 x 10^{-3} m^3/min. (2.5 slm and 10 slm). These parameters provide SiO$_2$ deposition rates of about 500 nm/min. (5,000 Angstroms/min) to 1000 nm/min (10,000 Angstroms/min). Typically, $0.4 \leq d \leq 1$ cm.

Presently preferred operating parameters for the PECVD oxide deposition step for a 0.15m (6 in) wafer are 10x10^{-6} m^3/s (600 sccm) oxygen, 15.0x10^{-6} m^3/s (900 sccm helium), 266.7x10^{-6} m^3/s (16,000 sccm) total flow (including purge; 25.0x10^{-6} m^3/s (1,500 sccm) excluding the purge), 1333.2±266.6Pa (10 ± 2 torr) pressure and 375°C ± 20°C wafer temperature. The parameters provide SiO$_2$ deposition rates of about 8,500 Angstroms/min. for a gas distributor-to-wafer surface distance, d = 0.004m 0.4 cm.

Quite obviously, the above-described high pressure, PECVD oxide deposition process, which is based upon TEOS gas chemistry and has essentially the same chamber requirements as the crucial conformal silicon dioxide deposition step, makes the use of the same chamber not only possible, but preferable.

There are several methods known in the art for depositing silicon dioxide by chemical vapor deposition, including the use of silane and oxygen and pyrolysis of tetraethylorthosilicate (TEOS) at a temperature in the range of 700 to 800°C at a pressure less than about 666.6Pa (5 Torr). This pyrolysis process may be utilized, with a silicon nitride, silane and ammonia plasma, or with an oxynitride, silane, ammonia and N$_2$O plasma. Plasma-assisted chemical vapor depositions using TEOS at pressures below 1 Torr are also utilized, with variations including use of spin on glass, and polyimides.

The present PECVD process provides methods for improving deposition rate, cracking resistance, physical and electrical properties of CVD-deposited silicon dioxide. The present invention also provides an improved method for depositing silicon dioxide whereby improved step coverage and lower stress of the deposited layer are obtained.

In particular, the present PECVD process provides an improved method for the plasma-enhanced chemical vapor deposition of TEOS to obtain the above advantageous improvements whereby the preferred conditions of deposition are a higher than usual pressures (up to 6666.1 Pa (50 Torr)) and at temperatures of about 200 to 400°C. The usual conditions for the plasma-enhanced chemical vapor deposition using TEOS are at a total pressure range of up to about 1 Torr (including the carrier gas), of which the oxygen in the plasma is at a pressure of about 53.3 Pa (0.4 Torr). During deposition, the substrate temperature usually gradually increases from about room tempera-

ture to about 400°C. See, for example, Mackens et al., Thin Solid Films, 97:53-61 (1982).

The deposited silicon dioxide coatings according to the present invention also have improved cracking resistance and have improved step coverage over silicon dioxide coatings deposited by other methods. The problem of step coverage deals with the creation of a mushroom-shaped deposited overhang at the corners of the step substrate. This overhang must be removed by subsequent processing, thus complicating the process. By utilizing the process according to the present invention, the problem of the overhang is much less severe, thereby minimizing or even eliminating the amount of processing to remedy this problem.

The silicon dioxide coatings formed according to the present invention also exhibit lower stress and are characterized generally by indices of -IE9 (compression) to +IE9 (tension), with the preferred index being -IE8. Also, the coatings according to the present invention exhibit improved physical and electrical properties and that the density, refractive index, shrinkage parameters, rate of etching, breakdown voltages, flat band voltages, mobile ion contamination, pinhole densities and silicon oxide purity are improved.

Finally, by utilizing the process according to the present invention, particularly in the apparatus disclosed in the above-identified co-pending application, the operation at high pressures (presently up to about, 6666.1 Pa (50 Torr)) allows the plasma to be confined at the top of the substrate, thus making it less likely to contaminate the sides of the chamber and the surfaces on which deposits are not desired.

Preferably, the third step is a high rate isotropic etch process comprising the step of exposing the existing silicon dioxide surface to a plasma formed from fluorinate gas selected from CF$_4$, NF$_3$ and C$_2$F$_6$ in a doping gas such as helium to stabilize the plasma, in a chamber at a temperature in the range of about 100°C to 500°C and preferably 200°C to 400°C. (Helium and/or oxygen can be incorporated to form gases with the carbon.) The total gas chamber pressure for these gases will usefully be in the range of about 26.7 to 2666.4 Pa (200 mt to 20 torr). The preferred range is 66.7 to 1333.2 Pa (500 mt to 10 torr). The total gas flow rate of the plasma will be determinable by those skilled in the art. However, an operable range of 0.33x10^{-6} to 58.33x10^{-6} m^3/s (20 sccm to 3.5 slm) has been found useful for the apparatus disclosed in the referenced multiple process CVD/PECVD reactor. The preferred total gas flow rate is from about 2.83x10^{-6} to 20.83x10^{-6} m^3/s (170 sccm to 1.25 slm). The useful range for the NF$_3$ (or C$_2$F$_6$) gas flow is from about 0.17x10^{-6} m^3/s (10 sccm to 500 sccm), with the preferred range being from

about 1.17x10⁻⁶ to 3.33x10⁻⁶m³/s (70 to 200 sccm). The individual flow rate of the doping gas, usually helium, will be from about 0.17x10⁻⁶ to 58.33x10⁻⁶m³/s (10 sccm to 3.5 slm) and, preferably 1.67x10⁻⁶ to 16.7x10⁻⁶m³/s (100 sccm to 1 slm). RF power density of about 5000 - 1000 w/m² (0.5 -1 watts/cm²) was used, along with radiant power from the lamp module to provide the substrate temperature of < 500°C and the preferred temperature of 200°C - 400°C. A distance of d≥0.004m is used. Below 0.004m, plasma instability increases. Also, as d is increased above 0./01m, the etch may become too effective and etch other components.

At the relatively high temperatures used, it has been found that rapid accurate isotropic etching of the silicon dioxide is accomplished. Specifically, etching rates of from 0.83x10⁻⁹m/s (500 Angstroms per minute) to 16.7x10⁻⁹m/s (1 micron per minute) are obtained wherein the etching is isotropically performed and smooth.

While this isotropic etch process is also useful generally, for example, for forming metal contacts, it is particularly useful for providing profile control of SiO₂ setep-coverage layers, as described above. In particularly, this uniform high rate isotropic etch has the advantage of additionally planarizing the substantially planarized contour which results from the SiO₂ deposition.

This high rate isotropic etch step was done in-situ in the same reactor used for the two above-described silicon dioxide deposition steps. As a consequence, this preferred sequence provides an integrated in-situ three-step process for forming a planarized silicon dioxide layer even over non-planar layers incorporating small geometry steps, trenches, etc. In combination with the TEOS and ozone-based thermal CVD conformal oxide deposition step, the use of the high rate PECVD oxide deposition step and the high rate etching step, the ability to use the same chamber for all three steps provides a fast, high throughput planarization process which is also less susceptible to contamination and wafer damage and other problems which result when a wafer is handled repeatedly and switched from one chamber to another.

The use of the above-described three-step planarization process is shown schematically in FIGS. 18 and 19. As depicted in FIG. 18, the first step forms a relatively thick stepped layer 182 of silicon dioxide over the stepped topography 181 at a very high deposition rate. The second step is then used to form thereon conformal silicon dioxide layer 183, which is substantially planarized despite the underlying deep step 184. Finally, as shown in FIG. 19, the third, isotropic etch step quickly etches away the upper surface 185 to below the residual step topography 186, if any, in layer 183,

thereby providing a smooth planar surface 187 for subsequent layers.

In addition, while the above-described three-step in-situ process is a presently preferred embodiment of our planarization process for silicon dioxide, the ozone- and TEOS-based thermal CVD step (second step) can be used in combination with other initial dielectric coatings and other isotropic etch steps. For example, the ozone thermal CVD second step can be used to deposit a highly conformal silicon dioxide coating on silicon oxide or silicon nitride or silicon oxynitride or other dielectric layers formed by CVD or by other methods, and the resulting substantially planarized layer can be etched to a planar topography using other, preferably high rate, dry (e.g., plasma) or wet chemical isotropic etch methods.

E. Chamber Self-Cleaning

An isotropic chamber self-cleaning etch sequence has been done using fluorinated gas at a pressure of about 79.99 to 1333.2 Pa (600 mT to 10 torr), high RF power density of 10000-20000 w/m² (1-2 watts/cm²), distance, d,≈ 0.01m and the other parameters, including the gas flow rates, described above for the isotropic etch process. This process has been used to clean the referenced multi-step CVD/PECVD reactor. After depositing an ~ 5x10⁻⁶m (5μ) thick silicon dioxide film on a wafer, the chamber can be cleaned in about one minute.

F. Summary; Alternative Process Sequences

The following is a partial listing of some of the possible ways in which the above-described deposition, etch and self-cleaning steps can be used, alone and in combination.

First, the thermal CVD conformal-oxide deposition process using ozone, oxygen and TEOS can be used alone to planarize an existing dielectric which has been formed, for example, without perfect step coverage or with perfect step coverage on a non-perfect topography.

Secondly, the conformal oxide-forming thermal CVD step can be applied to existing dielectrics followed by an isotropic etch step to etch back any remaining non-planarities to a planar topography.

Third, in a preferred high rate planar-dielectric forming sequence which can be used by itself to form dielectrics such as inter-level dielectrics or can be applied to rectify imperfect step coverage and/or topography in existing dielectrics, the above-described high rate PECVD oxide step is applied followed by the conformal oxide-forming thermal CVD sequence. In a preferred sequence using isotropic etch back to remove any non-planar

features, the high rate PECVD oxide deposition sequence is utilized followed by the conformal oxide-forming thermal CVD step followed by an isotropic etch step, preferably the above-described high rate plasma isotropic etch.

Numerous other combinations are possible for particular situations/problems. For example, the following sequence may be preferred where it is desired to form a thin protective oxide layer over a sensitive device or other structure before the application of RF power:

1. Thermal O_3 CVD Conformal-Oxide Deposition;
2. High Rate PECVD Oxide Deposition;
3. Thermal O_3 CVD Conformal-Oxide Deposition;
4. PECVD Oxide Deposition; and
5. High Rate Isotropic Etch.

Also, for forming very thick planar oxides over stepped topographies, the first two steps of the following sequence can be used to planarize the stepped topography followed by application of the high rate oxide deposition to build up the very thick oxide thickness over the planar surface:

1. High Rate PECVD Oxide Deposition;
2. Thermal O_3 CVD Conformal Oxide Deposition; and
3. High Rate PECVD Oxide Deposition.

As another alternative, the very thick planar oxide process described immediately above can incorporate an isotropic etch back as the final step to achieve full planarization, and the required thickness.

Finally, but certainly not exhaustively, the isotropic chamber self-cleaning etch can be inserted as desired within or at the end of the other process sequences to maintain the chamber in a clean deposition-free state.

Claims

1. A TEOS-based, plasma enhanced, CVD process for depositing a film of a silcon oxide having improved step coverage onto a surface of a semiconductor wafer having small dimension stepped topographics, such wafer being positioned inside a vacuum chamber to receive the silicon oxide,
comprising the steps of:
    heating the wafer to a temperature in the range of 200°C-500°C;
    pressurizing the chamber to between 133.322 Pa to 6666 Pa (1 to 50 Torr);
    dispensing toward the wafer a gas mixture which includes an effective amount of tetraethylorthosilicate ("TEOS") from a dispensing area which is close to the wafer surface, the gas mixture being dispensed with a substantially uniform spatial distribution over the wafer surface; and
    applying an effective amount of RF power between the dispensing area and the wafer, so as to excite the gas mixture into a plasma state in a thin region between the wafer and the dispensing area;
    whereby a layer of silicon oxide having improved step coverage is deposited onto the wafer.

2. A process according to Claim 1, characterised in that oxygen is provided to the gas mixture at an oxygen flow rate between 100 X 10^{-6} m³/min. and 1000 X 10^{-6} m³/min. (100 and 1000 sccm) such that the total flow rate of the gas mixture is between 200 X 10^{-6} m³/min. and 2500 X 10^{-6} m³/min. (200 and 2500 sccm).

3. A process according to Claim 1 or Claim 2, characterised in that RF power is applied at a density of about 1 W/cm².

4. A process according to any of the preceding claims, characterised in that the RF power is supplied via terminals, one of the terminals for said RF power supply being coupled to said wafer.

5. A process according to any of the preceding claims, characterised in that the step of applying RF power is carried out at a frequency of approximately 13.56 MHz.

6. A process according to any of the preceding claims, characterised in that the step of applying said RF power includes confining the plasma to a region corresponding to a single wafer.

7. A process according to any of the preceding claims, characterised in that the gas mixture is dispensed from a generally planar dispensing area which is located close to and substantially parallel with the wafer surface.

8. The process according to Claim 7, characterised in that the surface area of said planar dispensing area is approximately equal to or greater than the surface area of said wafer surface.

9. A process according to any of the preceding claims, characterised in that the process includes the step of gasifying liquid TEOS.

10. A process according to any of the preceding claims, characterised in that the process includes the step of transporting the wafer to its

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position in the chamber close to and substantially parallel to the planar dispensing region.

11. A process as claimed in any one of the preceding claims, characterised in that the process includes the steps of: positioning the substrate on a support within a vacuum chamber; communicating the gas mixture onto the chamber to a first volume adjacent the substrate; directing the gas mixture from said first volume in a multiplicity of closely-spaced streams through a second volume between the first volume and the substrate while applying RF energy to the second volume: and maintaining the total pressure in the chamber within the range of 133.322 Pa to 6666 Pa (1 to 50 Torr) and the temperature of the substrate in the range of 200°C to 500°C.

12. A process according to Claim 11, characterised in that the chamber is pressurised to between 133.322 Pa to 1600 Pa (1 to 12 Torr).

13. The process according to Claim 11 or Claim 12, characterised in that said process includes the step of confining the plasma created to a region corresponding to a single wafer.

14. The process according to any of the preceding claims, characterised in that said dispensing step further comprises dispensing the gas mixture toward the wafer through a plurality of openings in an electrically conductive electrode, said dispensing electrode having a planar surface containing said openings which faces the wafer and which is substantially co-extensive with said planar dispensing area; and wherein the step of applying RF power further comprises electrically connecting a source of RF power to the dispensing electrode.

15. The process according to Claim 14, characterised in that the step of applying RF power further comprises electrically connecting said source of RF power between the dispensing electrode and the wafer.

16. The process according to any of the preceding claims, characterised in that the step of applying RF power further comprises the steps of mounting the wafer on a pedestal which contains an electrically conductive electrode, and electrically connecting a source of RF power to the pedestal electrode.

17. The process according to any of the preceding claims, characterised in that, during the dispensing and applying steps, the wafer surface

is positioned a short distance from the planar dispensing area, said short distance being much less than the diameter of the wafer.

18. The process according to Claim 17, characterised in that, prior to said dispensing and applying steps, the wafer is transported to a moveable pedestal and the pedestal is moved so that the wafer surface is substantially parallel to, and is said short distance from, the planar dispensing area.

19. The process according to any of the preceding claims, characterised in that the deposit of the silicon oxide onto the wafer is at a rate substantially greater than 40 nm/min. (400 Angstroms per minute).

20. The process according to Claim 19, characterised in that the deposit of the silicon oxide onto the wafer is at a rate grater than or equal to about 500 nm/min. (5000 Angstroms per minute).

Patentansprüche

1. Plasmagestütztes CVD-Verfahren auf TEOS-Basis zum Abscheiden eines Siliziumoxidfilms mit verbesserter Stufenabdeckung auf eine Oberfläche eines Halbleiterwafers, der Topographien mit Stufen kleiner Abmessungen aufweist, wobei der Wafer sich zur Aufnahme des Siliziumoxids in einer Vakuumkammer befindet, wobei das Verfahren die Schritte aufweist:
    - Erwärmung des Wafers auf eine Temperatur im Bereich von 200°C bis 500°C;
    - Schaffen eines Drucks von 133,332 Pa bis 6666 Pa (1 bis 50 Torr) in der Kammer ;
    - Abgabe eines Gasgemischs zu dem Wafer hin, das eine nutzbare Menge Tetraethylorthosilikat ("TEOS") enthält, von einem Abgabebereich nahe der Oberfläche des Wafers, wobei das Gasgemisch mit im wesentlichen gleichmäßiger räumlicher Verteilung über der Oberfläche des Wafers verteilt wird; und
    - Anlegen eines nutzbaren Betrags von HF-Energie zwischen dem Abgabebereich und dem Wafer, um so das Gasgemisch in einem dünnen Bereich zwischen dem Wafer und dem Abgabebereich in einen Plasmazustand anzuregen,
    - wodurch eine Siliziumoxidschicht mit verbesserter Stufenabdeckung auf dem Wafer abgeschieden wird.

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2. Verfahren nach Anspruch 1, dadurch **gekennzeichnet**, daß dem Gasgemisch Sauerstoff mit einem Volumenstrom zwischen 100 x 10⁻⁶ m³/min und 1000 x 10⁻⁶ m³/min (100 und 1000 sccm) hinzugefügt wird, so daß der Gesamtvolumenstrom des Gasgemisches zwischen 200 x 10⁻⁶ m³/min und 2500 x 10⁻⁶ m³/min (200 und 2500 sccm) liegt.

3. Verfahren nach Anspruch 1 oder 2, dadurch **gekennzeichnet**, daß HF-Energie mit einer Dichte von etwa 1 W/cm² angelegt wird.

4. Verfahren nach einem der vorhergehenden Ansprüche, dadurch **gekennzeichnet**, daß die HF-Energie über Klemmen eingespeist wird, wobei eine der Klemmen für das Einspeisen der HF-Energie mit dem Wafer gekoppelt ist.

5. Verfahren nach einem der vorhergehenden Ansprüche, dadurch **gekennzeichnet**, daß der Schritt des Anlegens von HF-Energie mit einer Frequenz von annähernd 13,56 MHz ausgeführt wird.

6. Verfahren nach einem der vorhergehenden Ansprüche, dadurch **gekennzeichnet**, daß der Schritt des Anlegens der HF-Energie eine Einschliessung des Plasmas auf einen einem einzigen Wafer entsprechenden Bereich einschließt.

7. Verfahren nach einem der vorhergehenden Ansprüche, dadurch **gekennzeichnet**, daß das Gasgemisch von einem insgesamt ebenen, sich nahe der Oberfläche des Wafers befindlichen und im wesentlichen zu ihr parallelen Angabebereich abgegeben wird.

8. Verfahren nach Anspruch 7, dadurch **gekennzeichnet**, daß der Oberflächenbereich des ebenen Abgabebereichs in etwa gleich dem Oberflächenbereich der Waferfläche oder größer ist.

9. Verfahren nach einem der vorhergehenden Ansprüche, dadurch **gekennzeichnet**, daß das Verfahren den Schritt der Verdampfung von flüssigem TEOS einschließt.

10. Verfahren nach einem der vorhergehenden Ansprüche, dadurch **gekennzeichnet**, daß das Verfahren den Schritt einschließt, daß der Wafer in der Kammer in seine Position nahe bei und im wesentlichen parallel zu dem ebenen Abgabebereich transportiert wird.

11. Verfahren nach einem der vorhergehenden Ansprüche, dadurch **gekennzeichnet**, daß das Verfahren folgende Schritte einschließt: Positionieren des Substrats auf einem Träger in einer Vakuumkammer; Einleiten des Gasgemisches in einen ersten, an das Substrat angrenzenden Raum in der Kammer; Leiten des Gasgemisches aus dem ersten Raum in einer Vielzahl von nahe beieinander befindlichen Strömen durch einen zweiten Raum zwischen dem ersten Raum und dem Substrat, wobei an dem zweiten Raum HF-Energie angelegt wird, sowie Beibehalten eines Gesamtdrucks in der Kammer im Bereich von 133,322 Pa bis 6666 Pa (1 bis 50 Torr) und einer Temperatur des Substrats im Bereich von 200°C bis 500°C.

12. Verfahren nach Anspruch 11, dadurch **gekennzeichnet**, daß in der Kammer ein Druck von 133,322 Pa bis 1600 Pa (1 bis 12 Torr) geschaffen wird.

13. Verfahren nach Anspruch 11 oder 12, dadurch **gekennzeichnet**, daß das Verfahren den Schritt einschließt, daß das erzeugte Plasma auf einem einem einzigen Wafer entsprechenden Bereich eingeschlossen wird.

14. Verfahren nach einem der vorhergehenden Ansprüche, dadurch **gekennzeichnet**, daß zu dem Schritt der Abgabe weiterhin gehört, daß das Gasgemisch durch eine Vielzahl von Öffnungen in einer elektrisch leitenden Elektrode zu dem Wafer hin abgegeben wird, wobei die Abgabeelektrode eine die Öffnungen enthaltende, ebene Oberfläche hat, die dem Wafer zugewandt ist und im wesentlichen die gleiche Erstreckung aufweist wie die ebene Abgabefläche, und wobei zu dem Schritt des Anlegens von HF-Energie weiterhin gehört, daß eine HF-Energiequelle elektrisch an die Abgabeelektrode angeschlossen wird.

15. Verfahren nach Anspruch 14, dadurch **gekennzeichnet**, daß zu dem Schritt des Anlegens von HF-Energie weiter gehört, daß die HF-Energiequelle elektrisch zwischen die Abgabeelektrode und den Wafer geschaltet wird.

16. Verfahren nach einem der vorhergehenden Ansprüche, dadurch **gekennzeichnet**, daß zu dem Schritt des Anlegens von HF-Energie die weiteren Schritte gehören, daß der Wafer auf einem eine elektrisch leitende Elektrode enthaltenden Sockel angebracht wird und daß eine HF-Energiequelle an die Sockelelektrode elektrisch angeschlossen wird.

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17. Verfahren nach einem der vorhergehenden Ansprüche, dadurch **gekennzeichnet**, daß die Waferoberfläche während der Schritte der Abgabe und des Anlegens in geringem Abstand von dem ebenen Abgabebereich positioniert wird, wobei der geringe Abstand viel kleiner ist als der Durchmesser des Wafers.

18. Verfahren nach Anspruch 17, dadurch **gekennzeichnet**, daß der Wafer vor den Schritten der Abgabe und des Anlegens zu einem beweglichen Sockel befördert wird und der Sockel so bewegt wird, daß die Waferoberfläche im wesentlichen parallel zu dem ebenen Abgabebereich ist und sich in dem geringem Abstand davon befindet.

19. Verfahren nach einem der vorhergehenden Ansprüche, dadurch **gekennzeichnet**, daß die Abscheidung des Siliziumoxids auf dem Wafer mit einer Geschwindigkeit von wesentlich mehr als 40 nm/min (400 Ångström pro Minute) erfolgt.

20. Verfahren nach Anspruch 19, dadurch **gekennzeichnet**, daß die Abscheidung des Siliziumoxids auf den Wafer mit einer Geschwindigkeit erfolgt, die größer als oder gleich 500 nm/min (5.000 Ångström pro Minute) ist.

Revendications

1. Procédé de dépôt chimique en phase vapeur, renforcé par plasma, à base de TEOS, pour déposer un film d'oxyde de silicium ayant une couverture de gradins améliorée sur une surface d'une tranche semiconductrice ayant une topographie en gradins de faible dimension, cette tranche étant placée à l'intérieur d'une chambre à vide pour recevoir l'oxyde de silicium, comprenant les étapes qui consistent :

à chauffer la tranche à une température dans la plage de 200°C-500°C ;

à mettre la chambre à une pression comprise entre 133,322 Pa et 6666 Pa (1 et 50 torrs) ;

à distribuer vers la tranche un mélange gazeux qui comprend une quantité efficace de tétraéthylorthosilicate ("TEOS") à partir d'une zone de distribution qui est proche de la surface de la tranche, le mélange gazeux étant distribué avec une distribution spatiale sensiblement uniforme sur la surface de la tranche ; et

à appliquer une valeur efficace de puissance RF entre la zone de distribution et la tranche, afin d'amener par excitation le mélange gazeux à un état de plasma dans une

région mince entre la tranche et la zone de distribution ;

grâce à quoi une couche d'oxyde de silicium ayant une couverture de gradins améliorée est déposée sur la tranche.

2. Procédé selon la revendication 1, caractérisé en ce que de l'oxygène est fourni au mélange gazeux à un débit d'écoulement d'oxygène compris entre $100 \times 10^{-6} m^3/min$ et $1000 \times 10^{-6} m^3/min$ (100 et 1000 sccm) de manière que le débit total d'écoulement du mélange gazeux soit compris entre $200 \times 10^{-6} m^3/min$ et $2500 \times 10^{-6} m^3/min$ (200 et 2500 sccm).

3. Procédé selon la revendication 1 ou la revendication 2, caractérisé en ce que de la puissance RF est appliquée à une densité d'environ 1 W/cm^2.

4. Procédé selon l'une quelconque des revendications précédentes, caractérisé en ce que l'alimentation en puissance RF passe par des bornes, l'une des bornes pour ladite alimentation en puissance RF étant couplée à ladite tranche.

5. Procédé selon l'une quelconque des revendications précédentes, caractérisé en ce que l'étape d'application de puissance RF est exécutée à une fréquence d'environ 13,56 MHz.

6. Procédé selon l'une quelconque des revendications précédentes, caractérisé en ce que l'étape d'application de ladite puissance RF consiste à confiner le plasma dans une région correspondant à une seule tranche.

7. Procédé selon l'une quelconque des revendications précédentes, caractérisé en ce que le mélange gazeux est distribué à partir d'une zone globalement plane de distribution qui est placée à proximité de la surface de la tranche et sensiblement parallèle à celle-ci.

8. Procédé selon la revendication 7, caractérisé en ce que l'aire de la surface de ladite zone plane de distribution est approximativement égale ou supérieure à l'aire de la surface de ladite tranche.

9. Procédé selon l'une quelconque des revendications précédentes, caractérisé en ce qu'il comprend une étape consistant à gazéifier du TEOS liquide.

10. Procédé selon l'une quelconque des revendications précédentes, caractérisé en ce qu'il

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comprend l'étape consistant à transporter la tranche jusqu'à sa position dans la chambre à proximité de, et sensiblement parallèlement à, la région plane de distribution.

11. Procédé selon l'une quelconque des revendications précédentes, caractérisé en ce qu'il comprend les étapes qui consistent : à positionner le substrat sur un support à l'intérieur d'une chambre à vide ; à communiquer le mélange gazeux à la chambre à un premier volume adjacent au substrat ; à diriger le mélange gazeux depuis ledit premier volume en une multitude de flux étroitement rapprochés à travers un second volume entre le premier volume et le substrat tout en appliquant de l'énergie RF au second volume ; et à maintenir la pression totale dans la chambre dans la plage de 133,322 Pa à 6666 Pa (1 à 50 torrs) et la température du substrat dans la plage de 200°C à 500°C.

12. Procédé selon la revendication 11, caractérisé en ce que la chambre est mise à une pression comprise entre 133,322 Pa et 1600 Pa (1 et 12 torrs).

13. Procédé selon la revendication 11 ou la revendication 12, caractérisé en ce qu'il comprend l'étape consistant à confiner le plasma engendré à une région correspondant à une seule tranche.

14. Procédé selon l'une quelconque des revendications précédentes, caractérisé en ce que ladite étape de distribution consiste en outre à distribuer le mélange gazeux vers la tranche à travers plusieurs ouvertures dans une électrode électriquement conductrice, ladite électrode de distribution ayant une surface plane contenant lesdites ouvertures, qui fait face à la tranche et qui est sensiblement de même étendue que ladite zone plane de distribution ; et dans lequel l'étape d'application de puissance RF consiste en outre à connecter électriquement une source de puissance RF à l'électrode de distribution.

15. Procédé selon la revendication 14, caractérisé en ce que l'étape d'application de puissance RF consiste en outre à connecter électriquement ladite source de puissance RF entre l'électrode de distribution et la tranche.

16. Procédé selon l'une quelconque des revendications précédentes, caractérisé en ce que l'étape d'application de puissance RF comprend en outre l'étape consistant à monter la

tranche sur un socle qui contient une électrode électriquement conductrice, et à connecter électriquement une source de puissance RF à l'électrode du socle.

17. Procédé selon l'une quelconque des revendications précédentes, caractérisé en ce que, pendant les étapes de distribution et d'application, la surface de la tranche est placée à une courte distance de la zone plane de distribution, ladite courte distance étant très inférieure au diamètre de la tranche.

18. Procédé selon la revendication 17, caractérisé en ce que, avant lesdites étapes de distribution et d'application, la tranche est transportée jusqu'à un socle mobile et le socle est déplacé de manière que la surface de la tranche soit sensiblement parallèle à, et se trouve à ladite courte distance de, la zone plane de distribution.

19. Procédé selon l'une quelconque des revendications précédentes, caractérisé en ce que le dépôt de l'oxyde de silicium sur la tranche s'effectue à une vitesse sensiblement supérieure à 40 nm/min (400 angströms par minute).

20. Procédé selon la revendication 19, caractérisé en ce que le dépôt de l'oxyde de silicium sur la tranche est effectué à une vitesse supérieure ou égale à environ 500 nm/min (5000 angströms par minute).
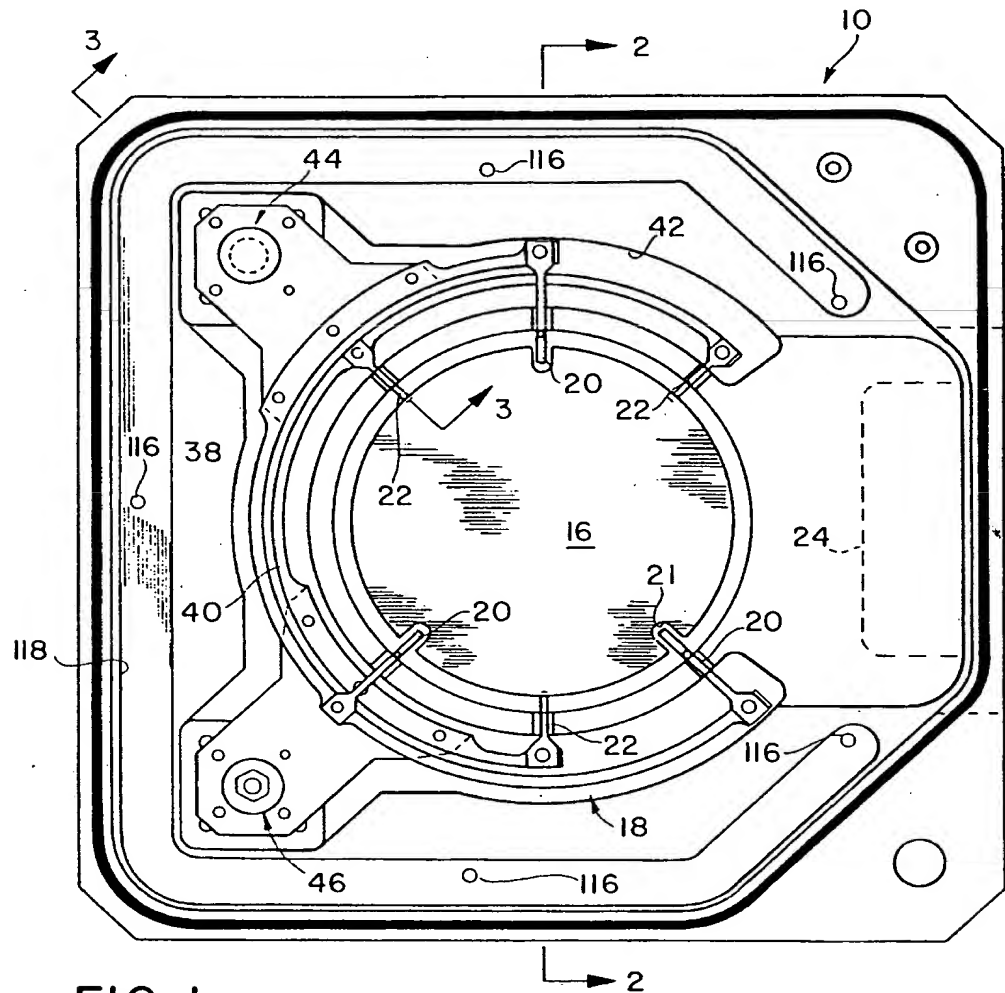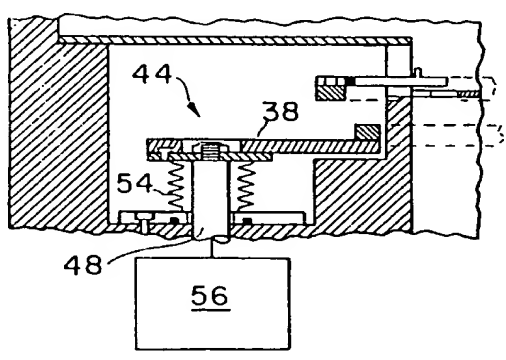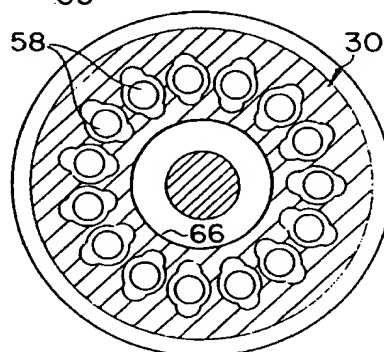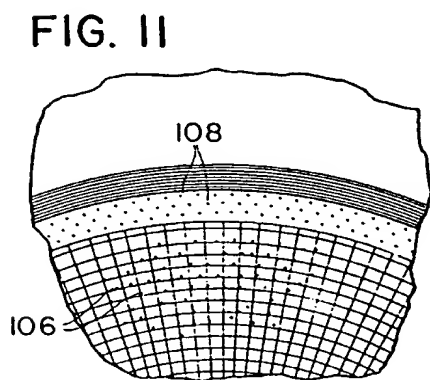
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FIG. I

FIG. 3

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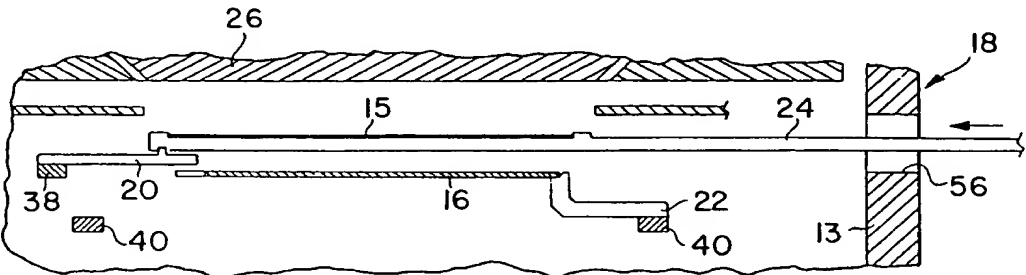
FIG. 2

FIG. II

FIG. 9
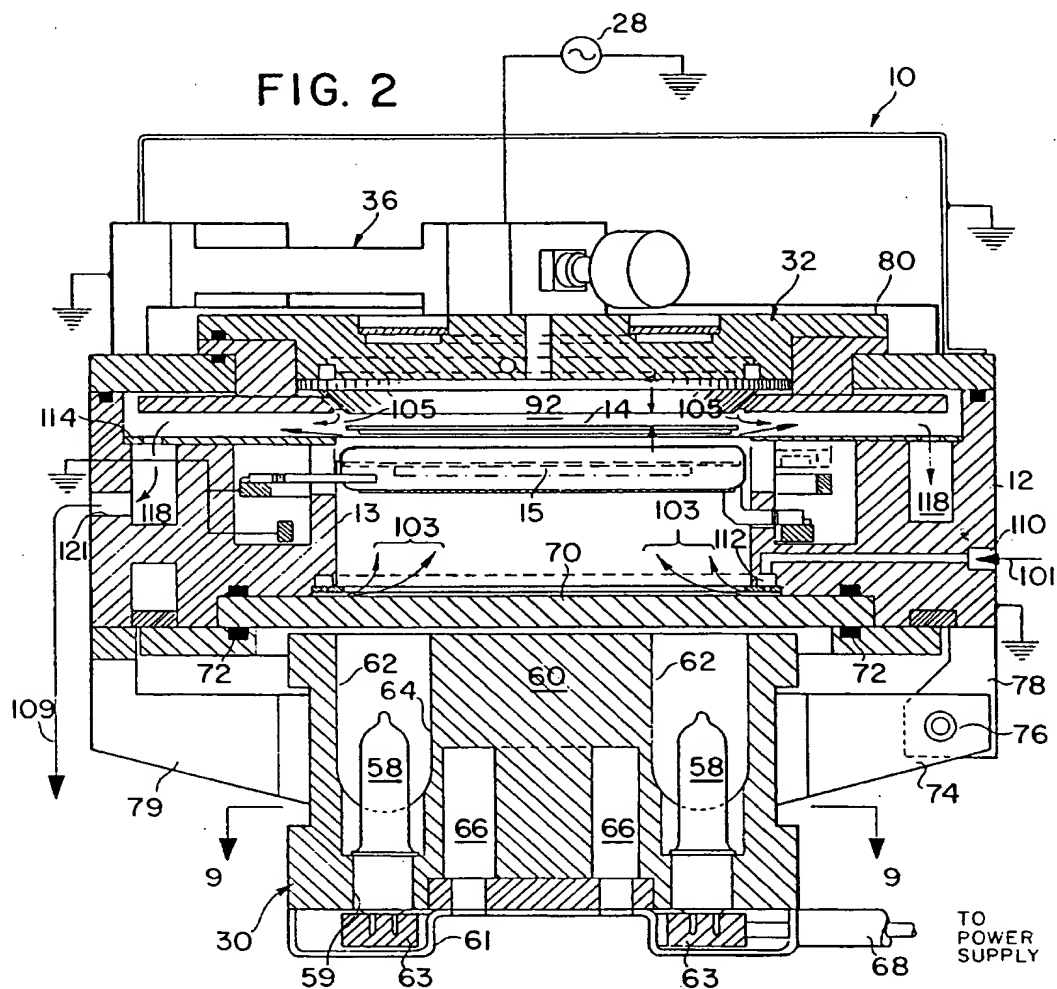
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FIG. 4
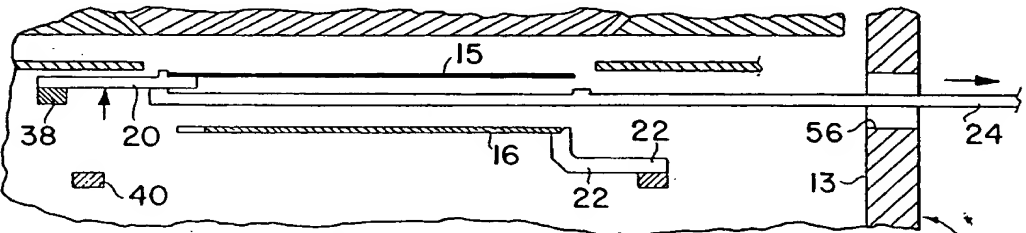
FIG. 5
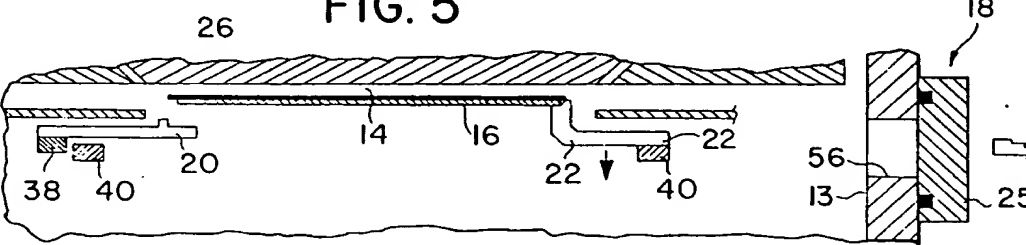
FIG. 6

FIG. 7

FIG. 8

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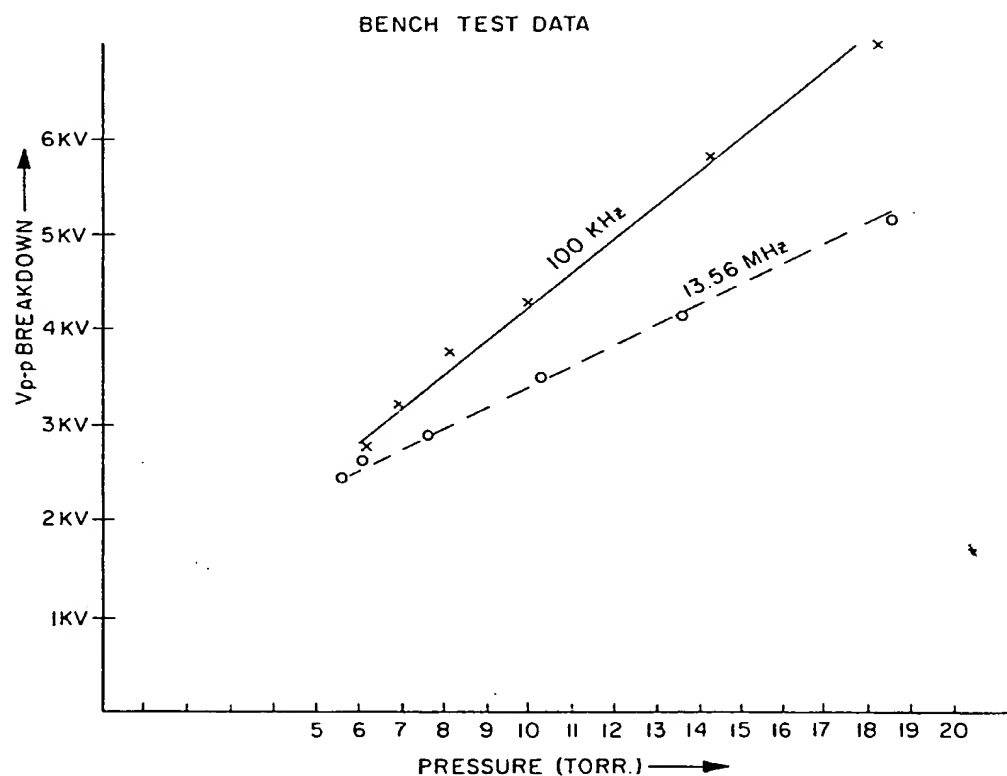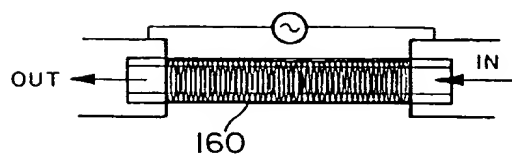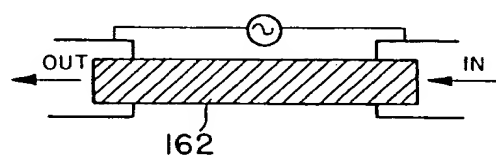
FIG. 12

FIG. 10

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BENCH TEST DATA
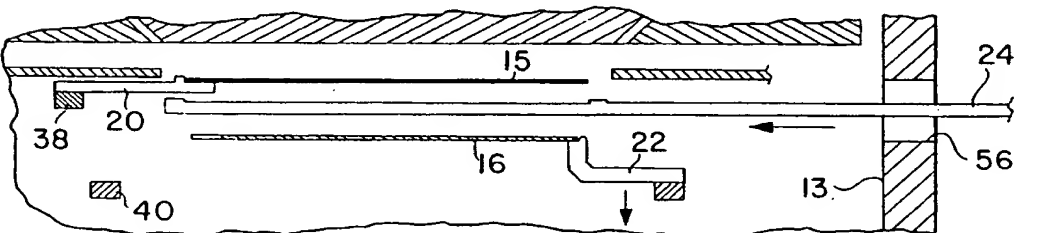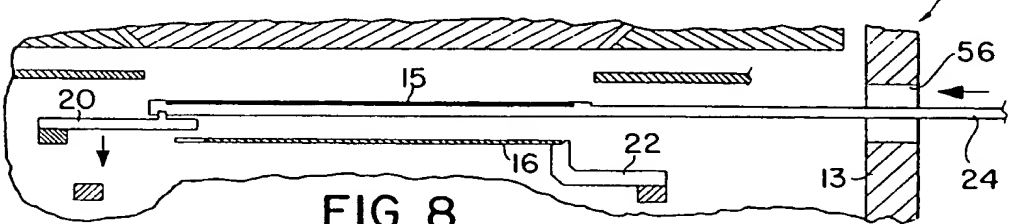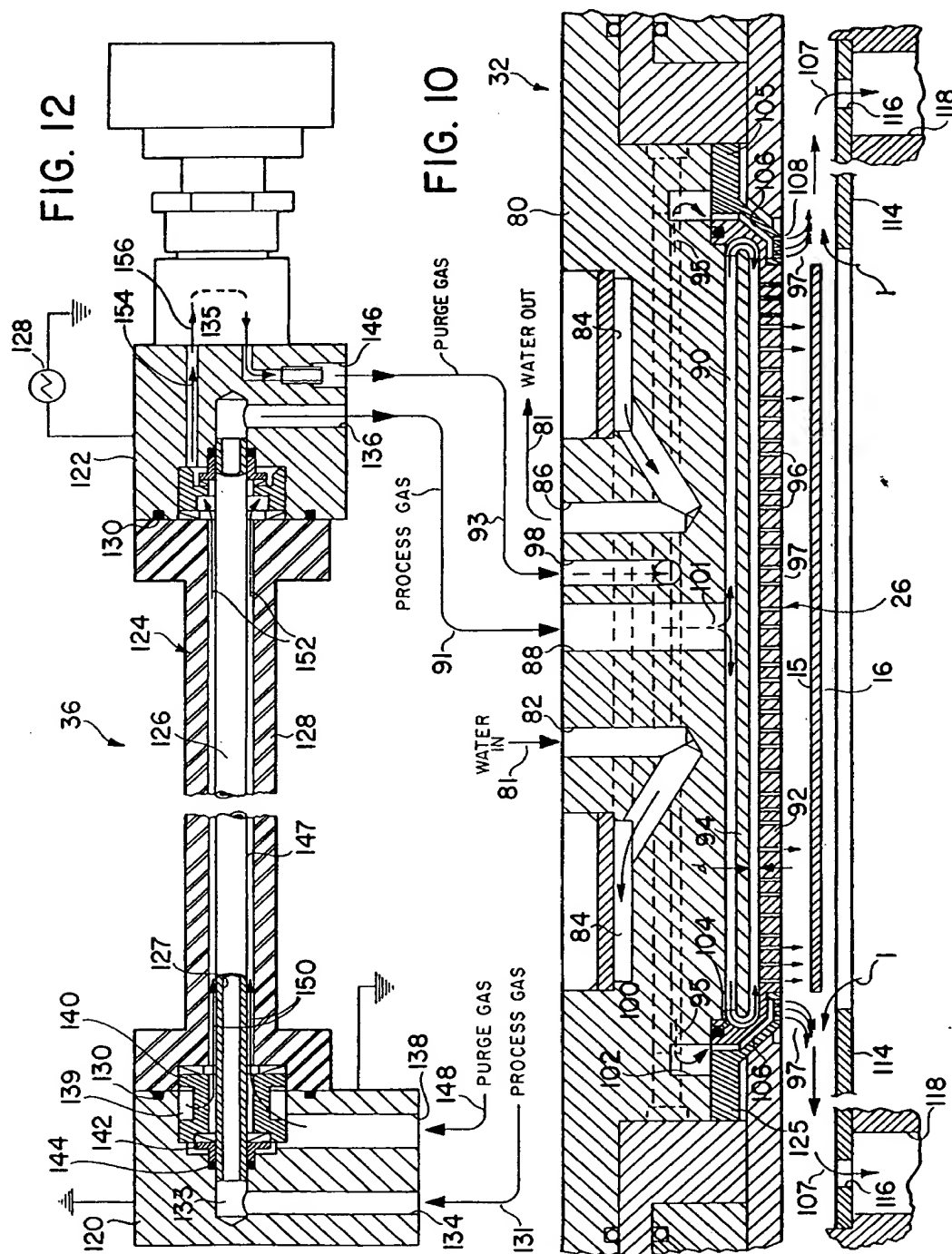
FIG. 14

FIG. 13A

FIG. 13B

FIG. 13C

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ELECTRICAL BREAKDOWN OF AIR AS A FUNCTION OF PRESSURE

FIG. 15

FIG. 16

FIG. 17A
PRIOR ART

FIG. 17B
PRIOR ART

FIG. 18

FIG. 19

FIG. 20

FIG. 21